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CPE 323: MSP430 LCD_A Controller

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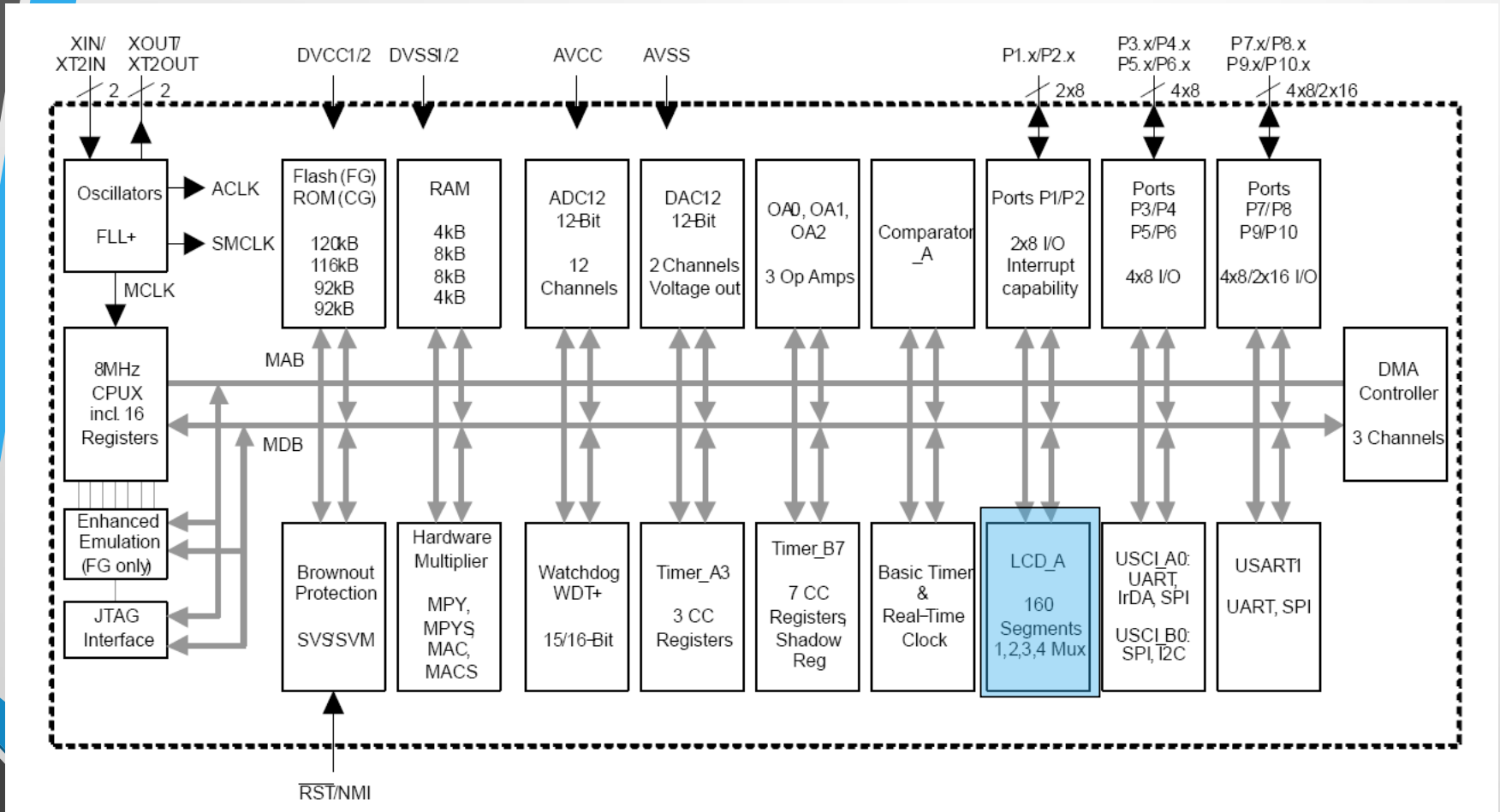
MSP430xG461x Microcontroller



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LCD Displays

- LCD - Liquid crystal display
  - Use much less power than LEDs
  - Does not emit light itself but controls the intensity of reflected or transmitted light
    - Backlight must be provided for a display to be used in dark surroundings
- Three classes
  - Segmented LCDs
  - Character-based LCDs
  - Fully graphical LCDs

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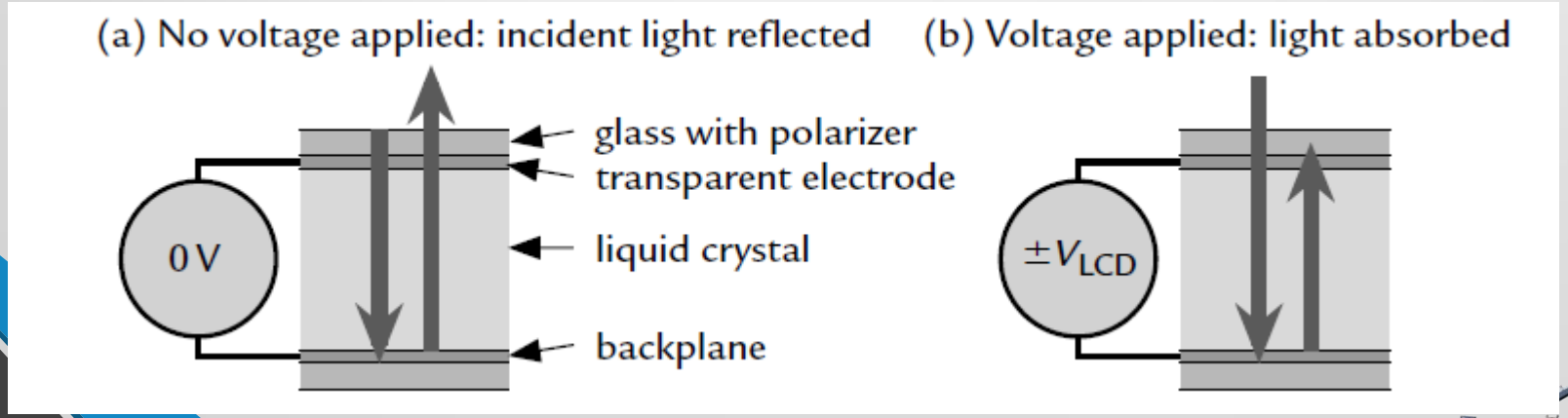
Reflective LCD: Operation Basics

- Construction: two glass plates carry transparent electrodes on their opposing faces and there is a mirror below the lower plate
  - Gap between is filled with a liquid crystal
- Bias voltage between electrodes = 0 =>
  Incident light is reflected and the display appears clear
- Sufficiently large bias voltage changes the optical properties of the liquid crystal so that reflected light is no longer transmitted through the upper glass and the segment appears dark
- Electrically the display is similar to a capacitor, albeit rather lossy

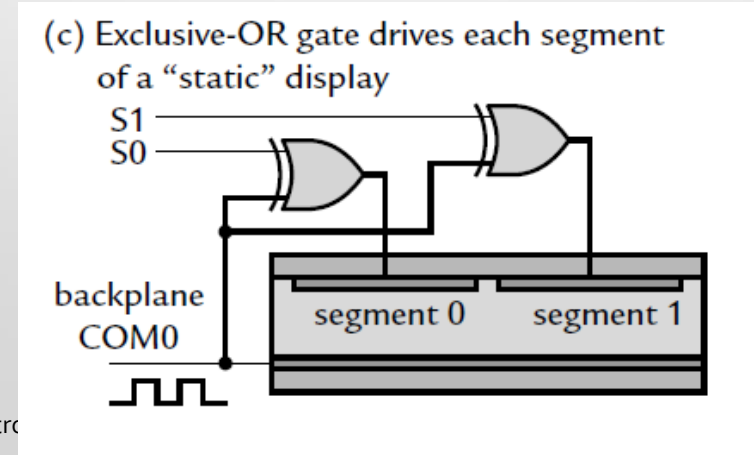


Reflective LCD: Operation Basics (cont'd)

- Complication: LCDs must be driven with AC, not DC
  - A steady voltage of only a few tens of millivolts leads to electrolysis of the liquid crystal, which eventually destroys the display
- Approach: The two electrodes of a segment are therefore driven with square waves in antiphase to produce an alternating voltage with zero mean
  - The frequency is low, typically around 100 Hz, but must not be close to multiples of the AC mains (line) frequency (50 or 60 Hz)
  - The output of many lights fluctuates at twice the frequency of the mains and the LCD appears to flicker if it is updated at a similar rate

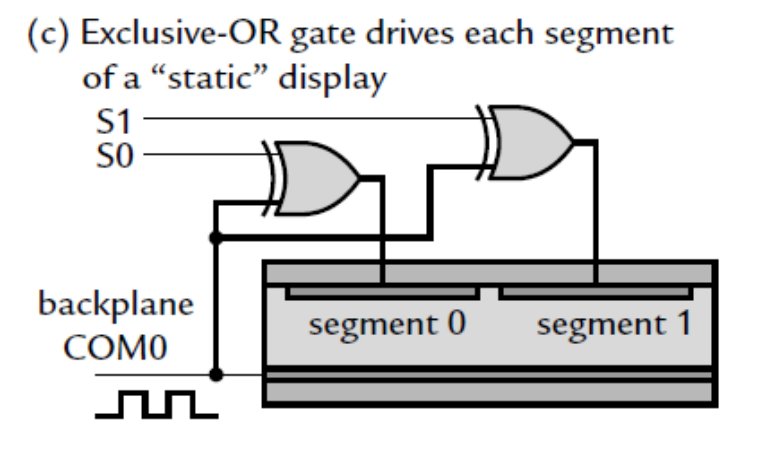
Driving Multiple Segments in LCDs

- Common backplane: COM - A square wave provides a clock to bias the display
- Each segment on the front has a separate connection: S0, S1
- An exclusive-OR gate with a control signal to each segment:
  - Si=0 => XOR gate transmits clock on COM0 unchanged => there is no potential difference between the electrodes, and the segment remains clear
  - Si=1 => XOR inverts the clock so that an alternating bias is applied to the segment, which turns dark
- XOR gates could be real devices but it is straightforward to implement this inside the MCU by toggling the outputs periodically



Driving Multiple Segments in LCDs (cont'd)

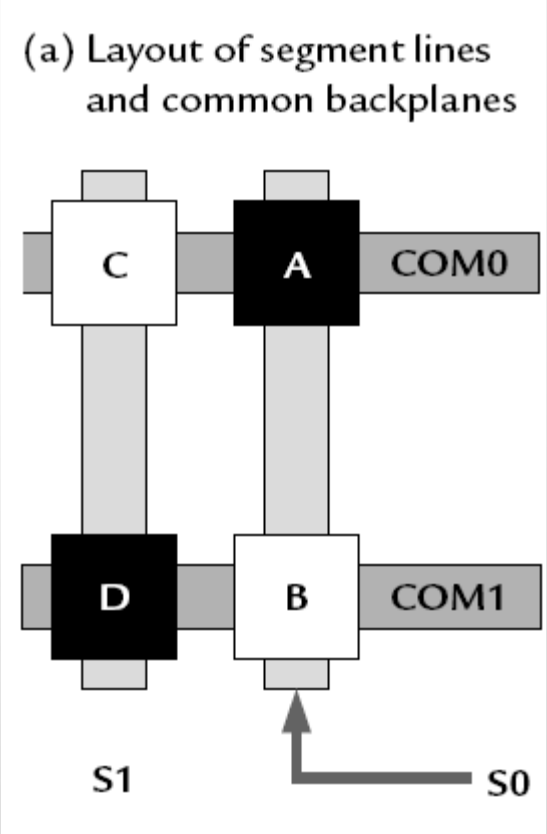
- Static approach:
  - One pin for each segment on display + one pin for backplane
  - Problem: Large number of pins



- Solution:
  - Multiplexed displays require fewer pins (multiple segments share a single pin)
  - Drawback: more trickier to multiplex LCDs because of the requirement for AC drive

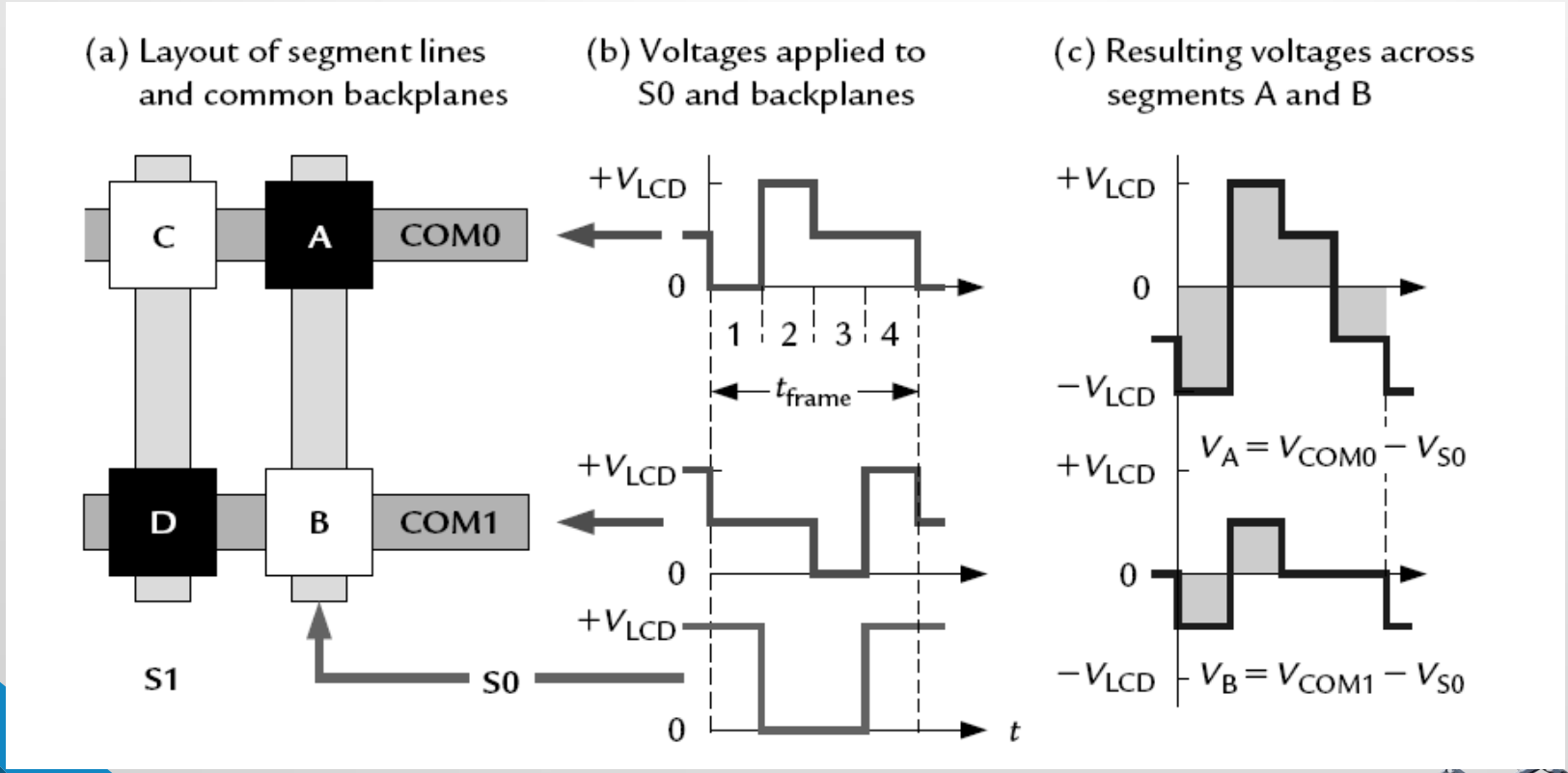
Two-way Multiplexing

- Example
  - 4 segments (A, B, C, and D)
  - 1 backplane
- Static: 5 pins
- Multiplexed: 4 pins
  - 2 common backplanes (COM0, COM1)
  - 2 signals (S0, S1)



Two-way Multiplexing

- Segment A: $V_{COM0} - V_{S0}$; Segment B: $V_{COM1} - V_{S0}$
- Segment C: $V_{COM0} - V_{S1}$; Segment D: $V_{COM1} - V_{S1}$



Two-way Multiplexing

- Each period of the waveforms, called a *frame, is divided into four phases:*
- 1. The segments on COM0 are addressed in the first phase by pulling COM0 to ground (0 V).
  - Segment A should be on and S0 is therefore driven to its maximum value, V_{LCD}
  - $V_A = V_{COM0} - V_{S0} = -V_{LCD}$
  - *The* segments on COM1 should be inactive during this phase and it is therefore put at a "neutral" voltage of $1/2V_{LCD}$
  - $V_B = V_{COM1} - V_{S0} = -1/2V_{LCD}$
- 2. The voltages in the second phase are the opposite of those in the first to ensure a pure AC signal with zero mean
  - $V_{COM0} = V_{LCD}$ *and* $V_{S0} = 0$ to give $V_A = +V_{LCD}$
  - *The backplane that is not being addressed,* COM1, remains at its neutral voltage of $1/2V_{LCD}$ *so that* $V_B = +1/2V_{LCD}$
- 3. Now it is the turn of COM1 to be addressed so it is pulled to ground and COM0 is set to neutral $1/2V_{LCD}$
  - Segment B should be off and S0 is therefore pulled to ground as well
- 4. This is the opposite of phase 3 to ensure that the mean voltage remains 0.

Two-way Multiplexing

- It is not possible to apply either the maximum voltage $\pm V_{LCD}$ *at all times to segments that should* be on nor a constant value of 0 to those that should be off
- Response of a segment depends on the root mean square (rms) value of the bias across it
- Suppose that $V_{LCD} = 3.0$ *V.* Then the values here are
  - *Vrms A* = $\sqrt{5/8}\ V_{LCD} \approx 2.4V$
  - *Vrms B* = $\sqrt{1/8}\ V_{LCD} \approx 1.1$ *V*
- The rms voltages have a ratio of $\sqrt{5}$ and are sufficiently large and small to make the segments dark and clear, respectively
- The drive is no longer purely “digital” because a voltage of 1/2 V_{LCD} is needed

LCD_A Display Clock

- Refresh rate: 30 Hz or faster to avoid flicker
  - Higher frequencies give a clearer display but consume more current
- 2-way multiplexed: 2x2, 4 clocks per frame
- 4-way multiplexed display needs eight clock cycles per frame (4x2)
  - fLCD must be at least 240 Hz
  - ACLK is at the usual 32 KHz =>
    32 K/240 = 136 or less,
    so a factor of 128 would probably be chosen

LCD_A Bias Voltage

- LCD_A has an internal chain of resistors
  - No external components are needed other than the display itself
  - An external resistor chain can be used to reduce the current required. A variable resistor can be attached as a contrast control

LCD_A Bias Voltage

- LCD_A offers three choices for the voltage to drive the display:
  - 1) Internal AVCC
  - 2) An external voltage, which may be used with either the internal or an external divider
  - 3) An internal charge pump, which provides an adjustable, regulated output in the range 2.60–3.44V, which can be controlled from software
    - A reservoir capacitor CLCD of at least 4.7F for the charge pump must be connected to the LCDCAP pin
    - Note: CPU may operate on low voltages

LCD_A Controller

- Liquid Crystal Display (LCD) controller
  - Included in several devices of the MSP430 families (’3xx and ’4xx)
  - Allows a rapid and simple way to interface with the program
- LCD controller commands the LCD panels generating voltage signals to the segments
- Features
  - Display memory
  - Automatic signal generation
  - Configurable frame frequency
  - Blinking capability
  - Support for 4 types of LCDs:
    - Static
    - 2-mux, 1/2 bias
    - 3-mux, 1/3 bias
    - 4-mux, 1/3 bias

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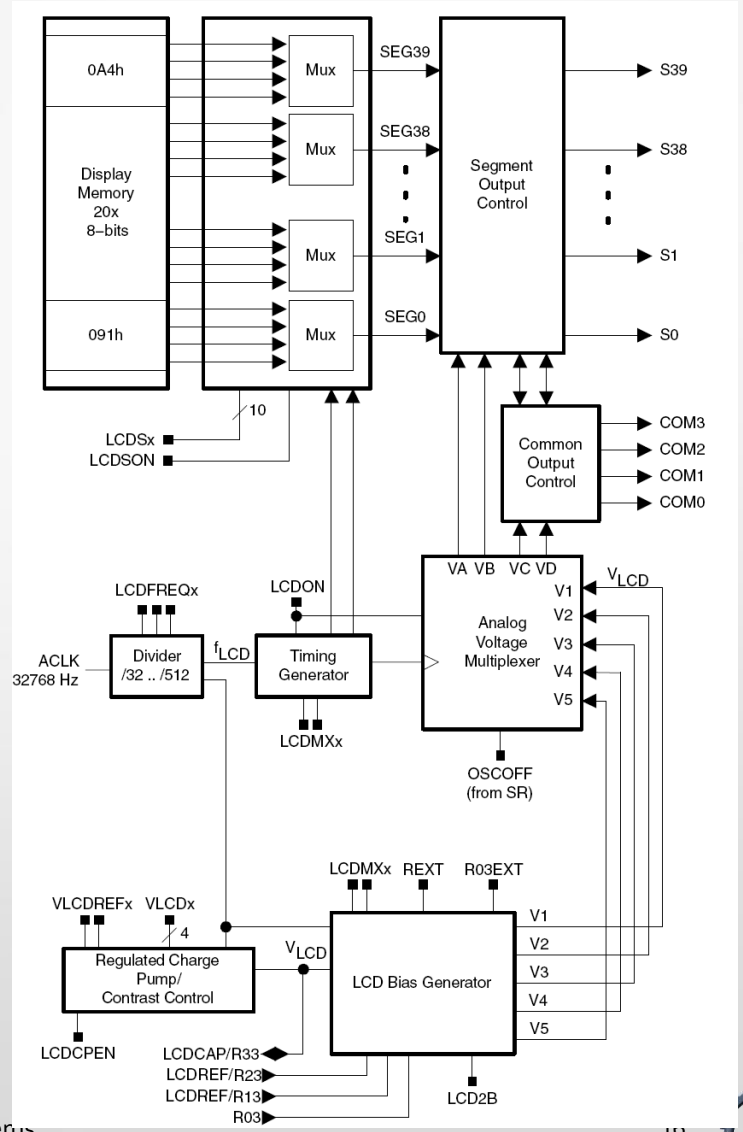
LCD_A Controller

Block Diagram



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LCD Memory Map

- Each memory bit corresponds to one LCD segment, or is not used, depending on the mode
- To turn on an LCD segment, its corresponding memory bit is set

Associated Common Pins	3	2	1	0	3	2	1	0		
Address	7							0	n	Associated Segment Pins
0A4h	--	--	--	--	--	--	--	--	38	39, 38
0A3h	--	--	--	--	--	--	--	--	36	37, 36
0A2h	--	--	--	--	--	--	--	--	34	35, 34
0A1h	--	--	--	--	--	--	--	--	32	33, 32
0A0h	--	--	--	--	--	--	--	--	30	31, 30
09Fh	--	--	--	--	--	--	--	--	28	29, 28
09Eh	--	--	--	--	--	--	--	--	26	27, 26
09Dh	--	--	--	--	--	--	--	--	24	25, 24
09Ch	--	--	--	--	--	--	--	--	22	23, 22
09Bh	--	--	--	--	--	--	--	--	20	21, 20
09Ah	--	--	--	--	--	--	--	--	18	19, 18
099h	--	--	--	--	--	--	--	--	16	17, 16
098h	--	--	--	--	--	--	--	--	14	15, 14
097h	--	--	--	--	--	--	--	--	12	13, 12
096h	--	--	--	--	--	--	--	--	10	11, 10
095h	--	--	--	--	--	--	--	--	8	9, 8
094h	--	--	--	--	--	--	--	--	6	7, 6
093h	--	--	--	--	--	--	--	--	4	5, 4
092h	--	--	--	--	--	--	--	--	2	3, 2
091h	--	--	--	--	--	--	--	--	0	1, 0
	Sn+1				Sn					

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LCD Controller Operation

- LCD controller supports blinking
  - The LCDSON bit is ANDed with each segment's memory bit.
    - When LCDSON = 1, each segment is on or off according to its bit value
    - When LCDSON = 0, each LCD segment is off
- Timing generation
  - Uses the f_{LCD} signal to generate the timing for common and segment lines
  - Proper frequency f_{LCD} depends on the LCD's requirement for framing frequency and LCD multiplex rate

LCD_A Voltage Generation

- Allows selectable sources for the peak output waveform voltage, V1, as well as the fractional LCD biasing voltages V2 – V5
- VLCD may be sourced from AVCC, an internal charge pump, or externally
- All internal voltage generation is disabled if the oscillator sourcing ACLK is turned off (OSCOFF = 1) or the LCD_A module is disabled (LCDON = 0)

LCD_A Voltage Selection

- Sourced from
  - AVCC when VLCDEXT = 0, VLCDx = 0, and VREFx = 0.
  - the internal charge pump when VLCDEXT = 0, VLCDPEN = 1, and VLCDx > 0
    - The charge pump is always sourced from DVCC
    - The VLCDx bits provide a software selectable LCD voltage from 2.6 V to 3.44 V (typical) independent of DVCC
    - The internal charge pump may use an external reference voltage when VLCDREFx = 01. In this case, the charge pump voltage will be 3x the voltage applied externally to the LCDREF pin and the VLCDx bits are ignored.
  - When VLCDEXT = 1, VLCD is sourced externally from the LCDCAP pin and the internal charge pump is disabled.

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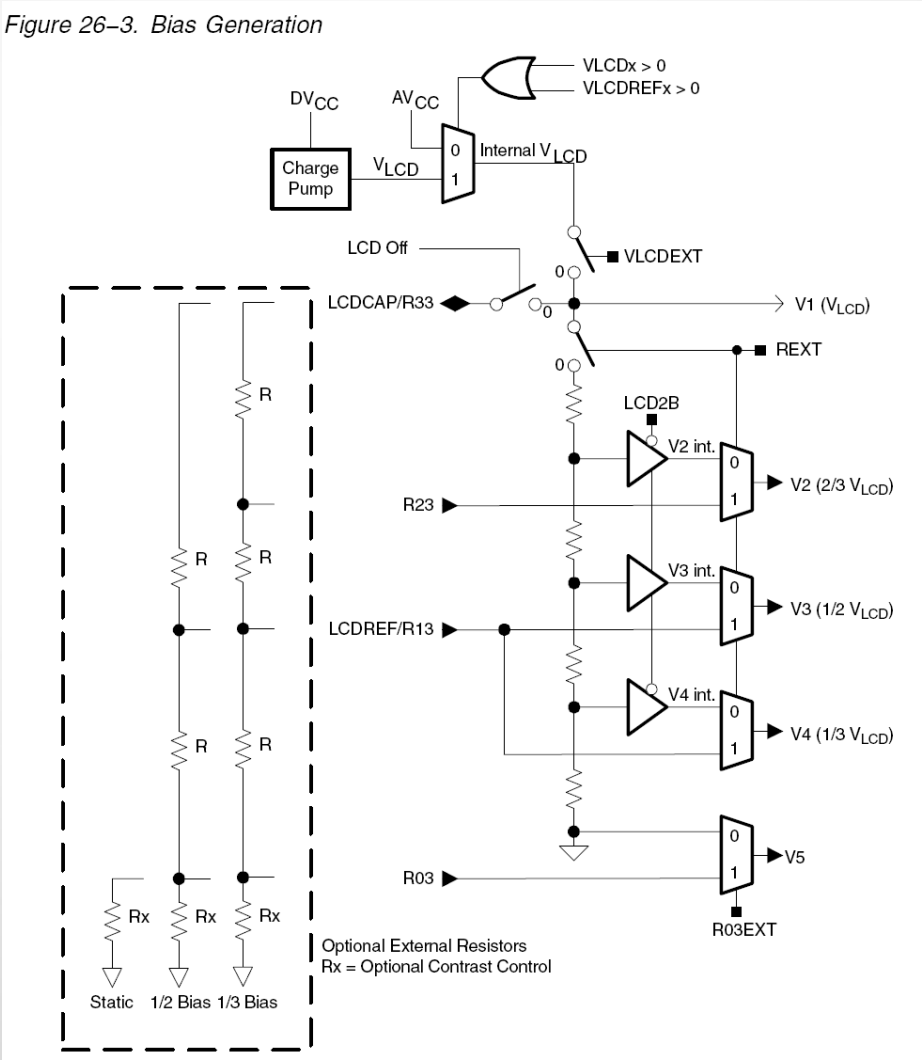
Bias Generation

- The fractional LCD biasing voltages, V2 – V5 can be generate internally or externally, independent of the source for VLCD
- REXT bit

Figure 26–3. Bias Generation



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LCD_A Voltage Generation

- The contrast ratio depends on the used LCD display and the selected biasing scheme
- Table 26−1 shows the biasing configurations that apply to the different modes together with the RMS voltages for the segments turned on (VRMS,ON) and turned off (VRMS,OFF) as functions of VLCD. It also shows the resulting contrast ratios between the on and off states

Table 26−1.LCD Voltage and Biasing Characteristics

Mode	Bias Config	LCDMx	LCD2B	COM Lines	Voltage Levels	$V_{RMS,OFF}/V_{LCD}$	$V_{RMS,ON}/V_{LCD}$	Contrast Ratio $V_{RMS,ON}/V_{RMS,OFF}$
Static	Static	00	X	1	V1, V5	0	1	1/0
2−mux	1/2	01	1	2	V1, V3, V5	0.354	0.791	2.236
2−mux	1/3	01	0	2	V1, V2, V4, V5	0.333	0.745	2.236
3−mux	1/2	10	1	3	V1, V3, V5	0.408	0.707	1.732
3−mux	1/3	10	0	3	V1, V2, V4, V5	0.333	0.638	1.915
4−mux	1/2	11	1	4	V1, V3, V5	0.433	0.661	1.528
4−mux	1/3	11	0	4	V1, V2, V4, V5	0.333	0.577	1.732

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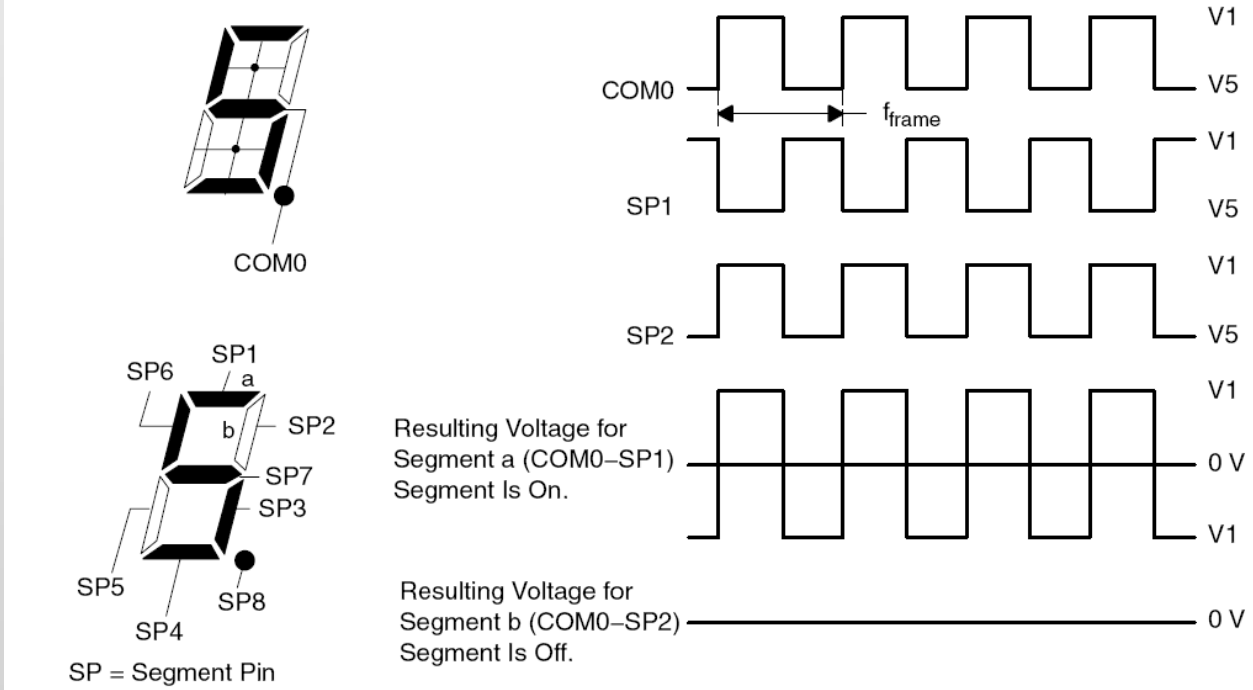
Static Mode

- Each MSP430 segment pin drives one LCD segment
- One common line, COM0, is used

Figure 26–4. Example Static Waveforms



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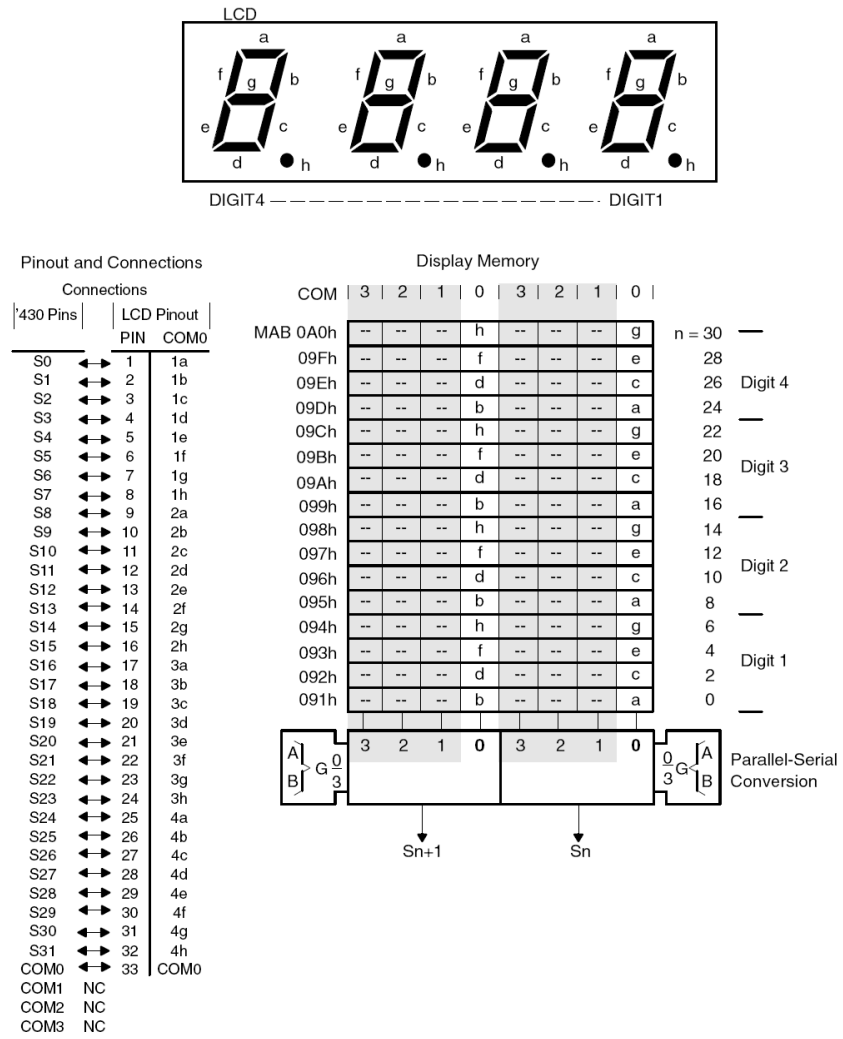
Static LCD Example

Figure 26–5. Static LCD Example



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Static Mode Software Example

```
;  All eight segments of a digit are often located in four
;  display memory bytes with the static display method.
;
a      EQU    001h
b      EQU    010h
c      EQU    002h
d      EQU    020h
e      EQU    004h
f      EQU    040h
g      EQU    008h
h      EQU    080h
;  The register content of Rx should be displayed.
:  The Table represents the 'on'-segments according to the
;  content of Rx.
       MOV.B  Table (Rx),RY    ; Load segment information
                               ; into temporary memory.
                               ; (Ry) = 0000 0000 hfdb geca
       MOV.B  Ry,&LCDn         ; Note:
                               ; All bits of an LCD memory
                               ' byte are written
       RRA    Ry               ; (Ry) = 0000 0000 0hfd bgec
       MOV.B  Ry,&LCDn+1       ; Note:
                               ; All bits of an LCD memory
                               ; byte are written
       RRA    Ry               ; (Ry) = 0000 0000 00hf dbge
       MOV.B  Ry,&LCDn+2       ; Note:
                               ; All bits of an LCD memory
                               ' byte are written
       RRA    Ry               ; (Ry) = 0000 0000 000h fdbg
       MOV.B  Ry,&LCDn+3       ; Note:
                               ; All bits of an LCD memory
                               ' byte are written


       ............
       ............
;
Table  DB     a+b+c+d+e+f      ; displays "0"
       DB     b+c;             ; displays "1"
       ............
       ............
       DB
       ............
```

h	f	d	b	g	e	c	a

h	f	d	b	g	e	c	a
o	h	f	d	b	g	e	c
o	o	h	f	d	b	g	e
o	o	o	h	f	d	b	g

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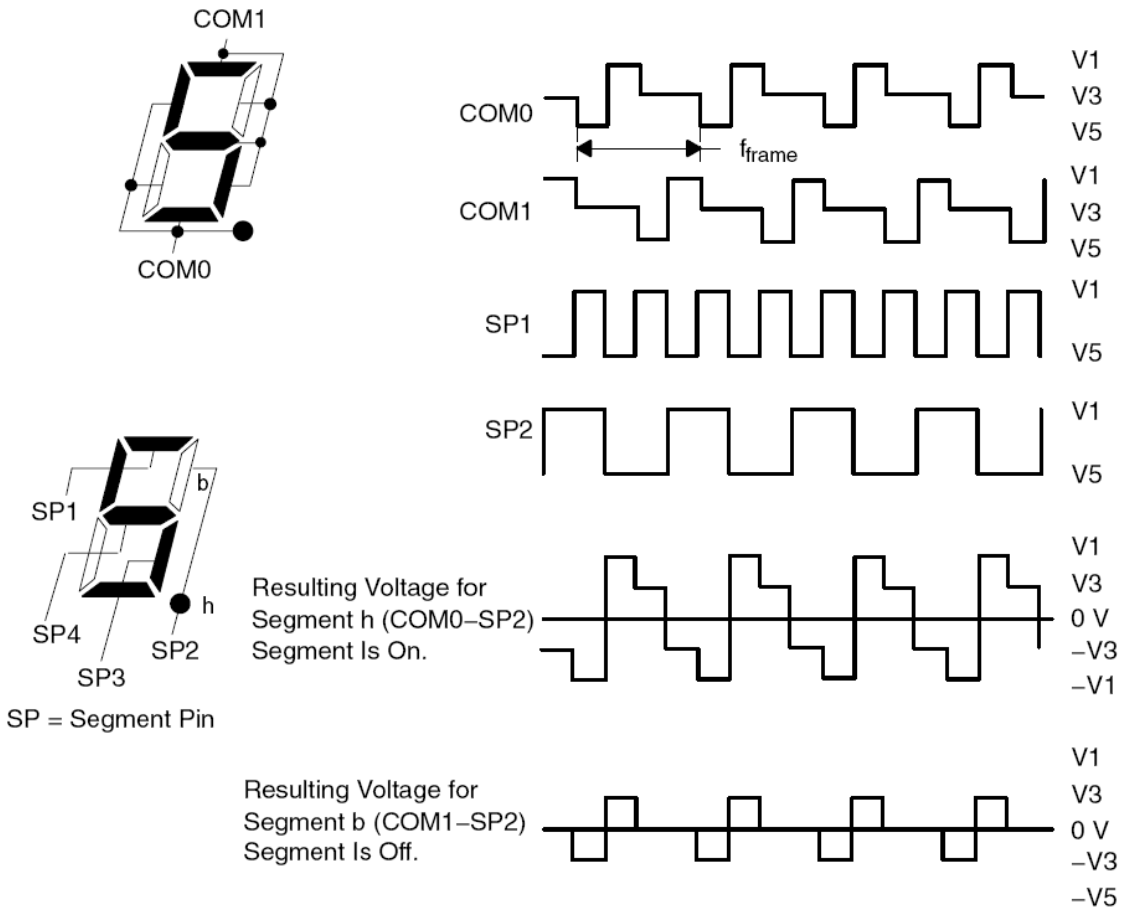
2-MUX Mode

- Each MSP430 segment pin drives two LCD segments
- Two common lines, COM0 and COM1, are used
- 2-mux example waveforms
  - *a=COM1-SP1*
  - *b=COM1-SP2*
  - *c=COM1-SP3*
  - *d=COM0-SP3*
  - *e=COM0-SP4*
  - *f=COM0-SP1*
  - *g=COM1-SP4*
  - *h=COM0-SP2*

Figure 26–6. Example 2-*Mux Waveforms*



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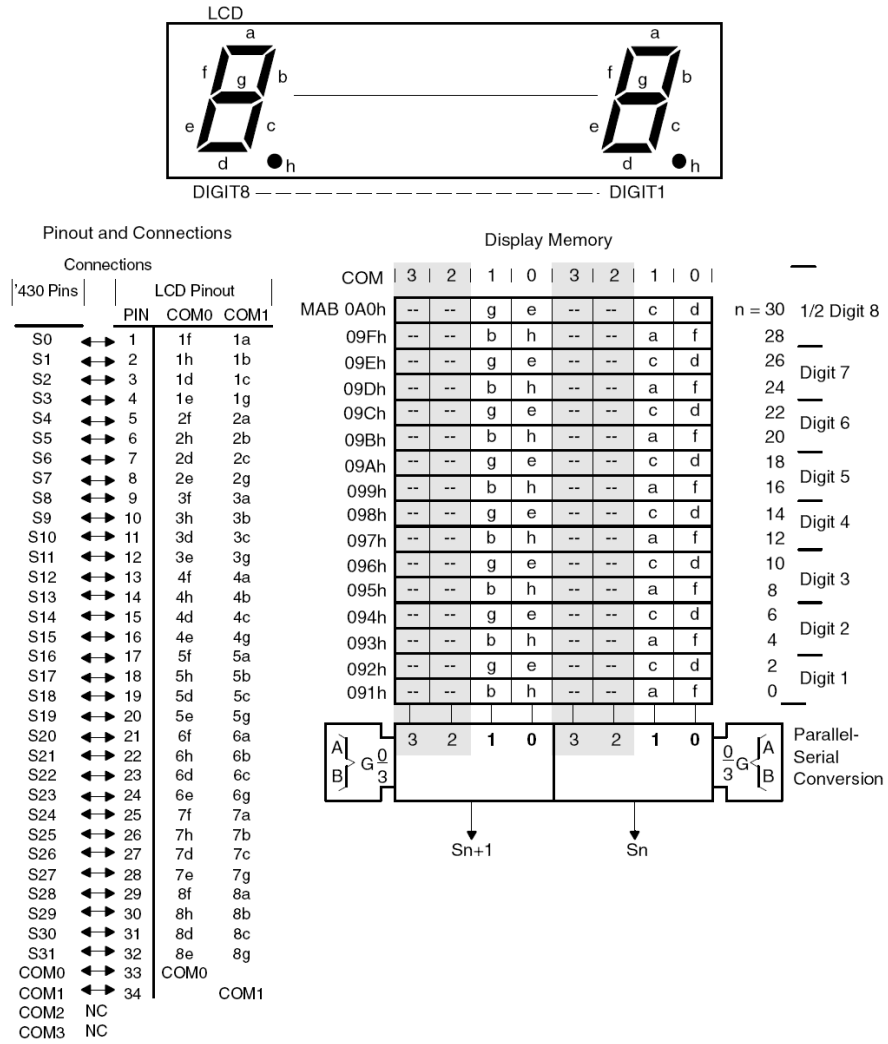
2-MUX LCD Example

Figure 26–7. 2–Mux LCD Example



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2-MUX Software Example

```
;  All eight segments of a digit are often located in two
;  display memory bytes with the 2mux display rate
;
a      EQU    002h
b      EQU    020h
c      EQU    008h
d      EQU    004h
e      EQU    040h
f      EQU    001h
g      EQU    080h
h      EQU    010h
;  The register content of Rx should be displayed.
;  The Table represents the 'on'-segments according to the
;  content of Rx.
;
       ...........
       ...........
       MOV.B  Table(Rx),Ry ; Load segment information into
                           ; temporary memory.
       MOV.B  Ry,&LCDn     ; (Ry) = 0000  0000  gebh  cdaf
                           ; Note:
                           ; All bits of an LCD memory byte
                           ; are written
       RRA    Ry           ; (Ry) = 0000  0000  0geb  hcda
       RRA    Ry           ; (Ry) = 0000  0000  00ge  bhcd
       MOV.B  Ry,&LCDn+1     ; Note:
                           ; All bits of an LCD memory byte
                           ; are written
       ...........
       ...........
       ...........
Table  DB     a+b+c+d+e+f     ; displays "0"
       ...........
       DB     a+b+c+d+e+f+g   ; displays "8"
       ...........
       ...........
       DB
       ...........
;
```


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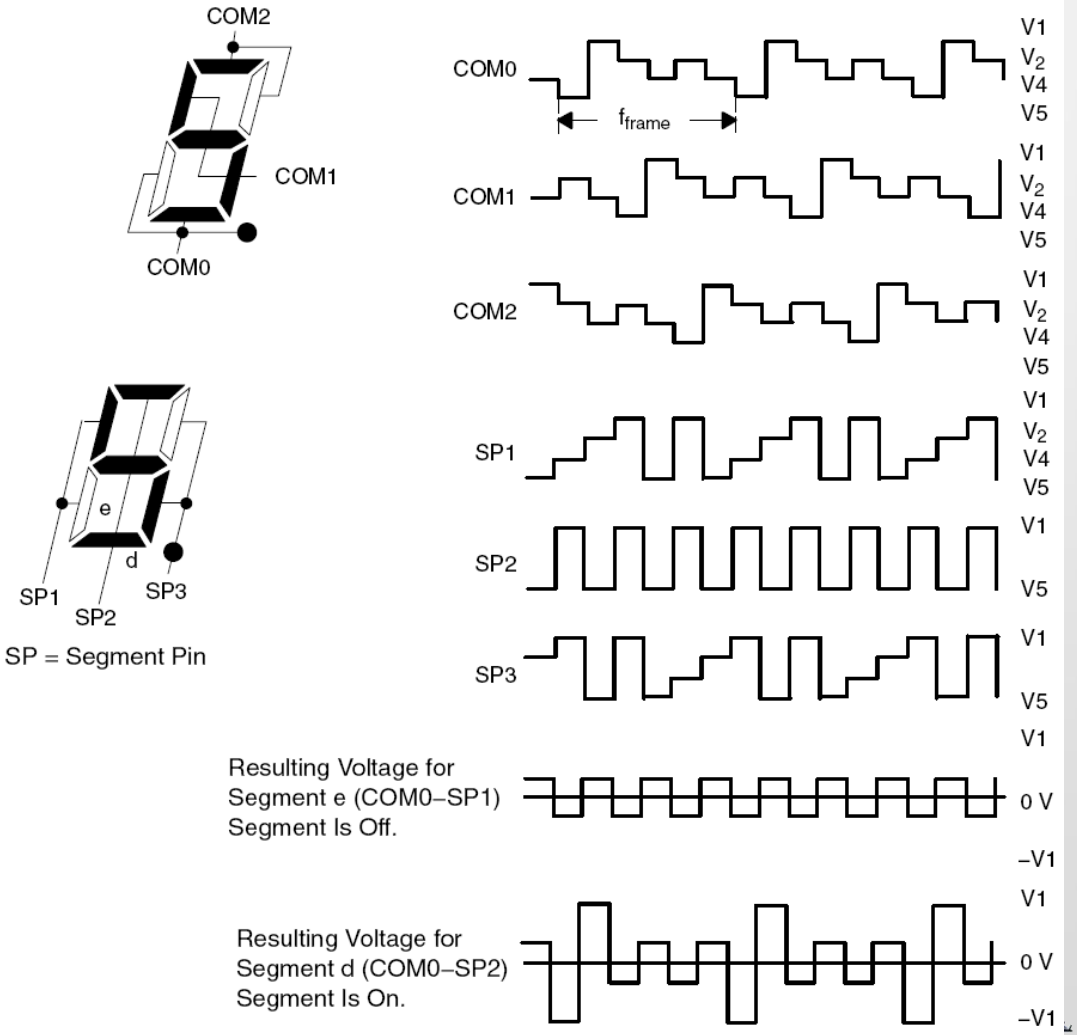
3-MUX Mode Waveforms

- Each MSP430 segment pin drives three LCD segments
- Three common lines, COM0 and COM1, and COM2 are used
- 3-mux example waveforms

Figure 26–8. Example 3-*Mux Waveforms*



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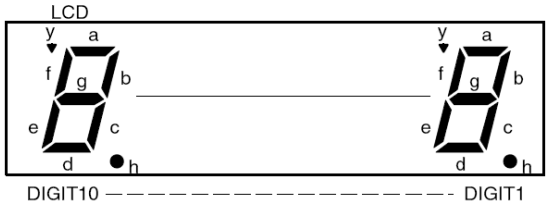
3-MUX LCD Example

Figure 26–9. 3-Mux LCD Example



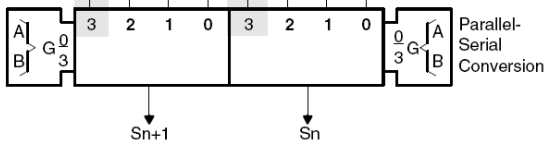
Pinout and Connections

Connections

'430 Pins		LCD Pinout PIN	COM0	COM1	COM2
S0	↔	1	1e	1f	1y
S1	↔	2	1d	1g	1a
S2	↔	3	1h	1c	1b
S3	↔	4	2e	2f	2y
S4	↔	5	2d	2g	2a
S5	↔	6	2h	2c	2b
S6	↔	7	3e	3f	3y
S7	↔	8	3d	3g	3a
S8	↔	9	3h	3c	3b
S9	↔	10	4e	4f	4y
S10	↔	11	4d	4g	4a
S11	↔	12	4h	4c	4b
S12	↔	13	5e	5f	5y
S13	↔	14	5d	5g	5a
S14	↔	15	5h	5c	5b
S15	↔	16	6e	6f	6y
S16	↔	17	6d	6g	6a
S17	↔	18	6h	6c	6b
S18	↔	19	7e	7f	7y
S19	↔	20	7d	7g	7a
S20	↔	21	7h	7c	7b
S21	↔	22	8e	8f	8y
S22	↔	23	8d	8g	8a
S23	↔	24	8h	8c	8b
S24	↔	25	9e	9f	9y
S25	↔	26	9d	9g	9a
S26	↔	27	9h	9c	9b
S27	↔	28	10e	10f	10y
S28	↔	29	10d	10g	10a
S29	↔	30	10h	10c	10b
COM0	↔	31	COM0		
COM1	↔	32		COM1	
COM2	↔	33			COM2
COM3	NC				

Display Memory

COM	3	2	1	0	3	2	1	0		
MAB 09Fh	--	a	g	d	--	y	f	e	n = 30	
09Eh	--	b	c	h	--	a	g	d	28	Digit 10
09Dh	--	y	f	e	--	b	c	h	26	Digit 9
09Ch	--	a	g	d	--	y	f	e	24	
09Bh	--	b	c	h	--	a	g	d	22	Digit 8
09Ah	--	y	f	e	--	b	c	h	20	Digit 7
099h	--	a	g	d	--	y	f	e	18	
098h	--	b	c	h	--	a	g	d	16	Digit 6
097h	--	y	f	e	--	b	c	h	14	Digit 5
096h	--	a	g	d	--	y	f	e	12	
095h	--	b	c	h	--	a	g	d	10	Digit 4
094h	--	y	f	e	--	b	c	h	8	Digit 3
093h	--	a	g	d	--	y	f	e	6	
092h	--	b	c	h	--	a	g	d	4	Digit 2
091h	--	y	f	e	--	b	c	h	2	Digit 1
									0	



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3-MUX Software Example

```
;  The 3mux rate can support nine segments for each
;  digit. The nine segments of a digit are located in
;  1 1/2 display memory bytes.
;
a      EQU    0040h
b      EQU    0400h
c      EQU    0200h
d      EQU    0010h
e      EQU    0001h
f      EQU    0002h
g      EQU    0020h
h      EQU    0100h
Y      EQU    0004h
;  The  LSDigit of register Rx should be displayed.
;  The Table represents the 'on'-segments according to the
;  LSDigit of register of Rx.
;  The register Ry is used for temporary memory
;
ODDDIGRLA    Rx            ; LCD in 3mux has 9 segments per
                           ; digit; word table required for
                           ; displayed characters.
       MOV   Table(Rx),Ry  ; Load segment information to
                           ; temporary mem.
                           ; (Ry) = 0000  0bch  0agd  0yfe
       MOV.B Ry,&LCDn      ; write 'a, g, d, y, f, e' of
                           ; Digit n (LowByte)
       SWPB  Ry            ; (Ry) =  0agd  0yfe  0000  0bch
       BIC.B #07h,&LCDn+1  ; write 'b, c, h' of Digit n
                           ; (HighByte)
       BIS.B Ry,&LCDn+1
       .....
EVNDIGRLA    Rx            ; LCD in 3mux has 9 segments per
                           ; digit; word table required for
                           ; displayed characters.
       MOV   Table(Rx),Ry  ; Load segment information to
                           ; temporary mem.
                           ; (Ry) = 0000  0bch  0agd  0yfe
       RLA   Ry            ; (Ry) = 0000  bch0  agd0  yfe0
       RLA   Ry            ; (Ry) = 000b  ch0a  gd0y  fe00
       RLA   Ry            ; (Ry) = 00bc  h0ag  d0yf  e000
       RLA   Ry            ; (Ry) = 0bch  0agd  0yfe  0000
       BIC.B #070h,&LCDn+1
       BIS.B Ry,&LCDn+1    ; write 'y, f, e' of Digit n+1
                           ; (LowByte)
       SWPB  Ry            ; (Ry) = 0yfe  0000  0bch  0agd
       MOV.B Ry,&LCDn+2    ; write 'b, c, h, a, g, d' of
                           ; Digit n+1 (HighByte)
       ...........
Table  DW    a+b+c+d+e+f   ; displays "0"
       DW    b+c           ; displays "1"
       ...........
       ...........
       DW    a+e+f+g       ; displays "F"
```


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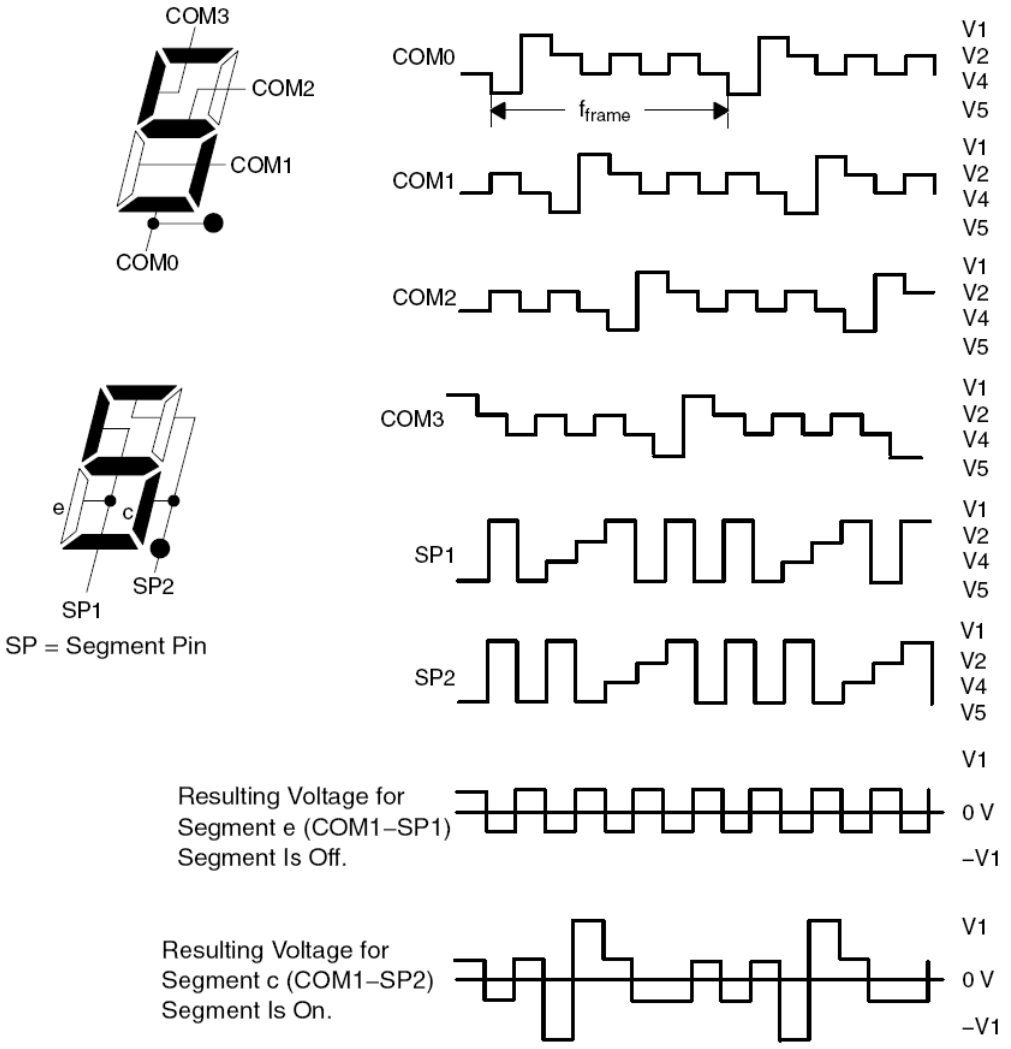
4-MUX Mode Waveforms

- Each MSP430 segment pin drives four LCD segments
- Four common lines, COM0, COM1, COM2, and COM3 are used
- 4-mux example waveforms

Figure 26–10. Example 4-*Mux Waveforms*



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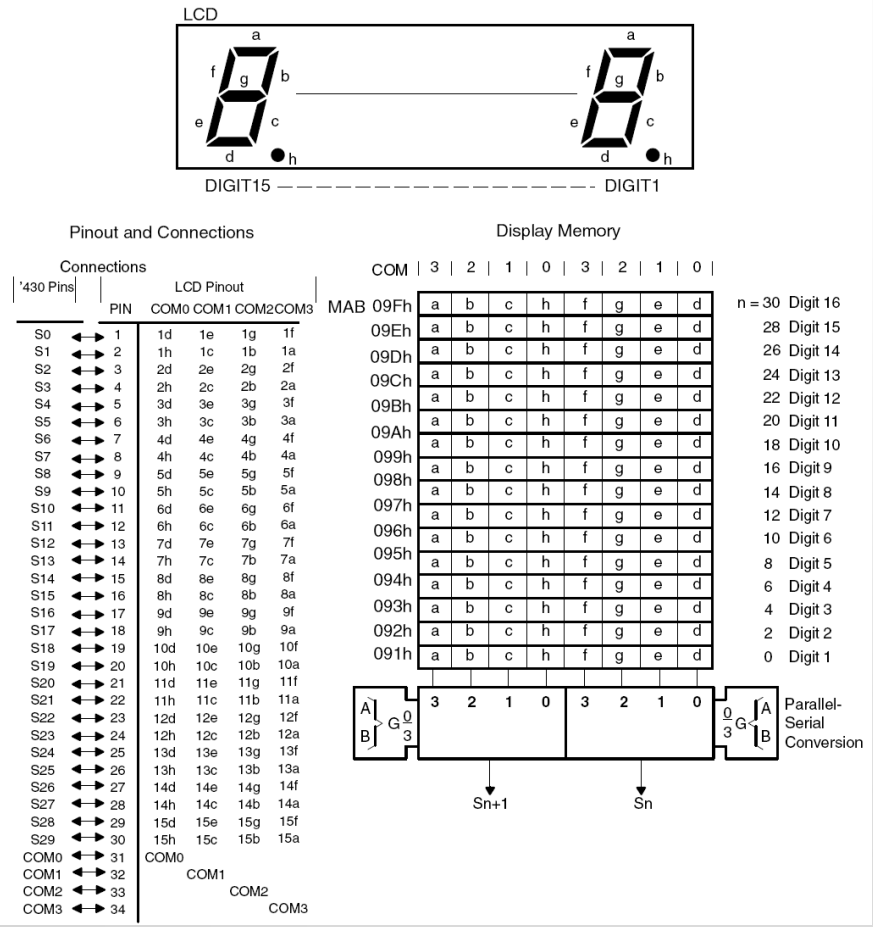
4-MUX LCD Example

Figure 26–11.4-Mux LCD Example



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4-MUX Software Example

```
;   The 4mux rate supports eight segments for each digit.
;   All eight segments of a digit can often be located in
;   one display memory byte
a       EQU     080h
b       EQU     040h
c       EQU     020h
d       EQU     001h
e       EQU     002h
f       EQU     008h
g       EQU     004h
h       EQU     010h
;
;   The  LSDigit of register Rx should be displayed.
;   The Table represents the 'on'-segments according to the
;   content of Rx.
;
        MOV.B  Table(Rx),&LCDn ; n = 1 ..... 15
                               ; all eight segments are
                               ; written to the display
                               ; memory
        ...........
        ...........

Table   DB      a+b+c+d+e+f    ; displays "0"
        DB      b+c            ; displays "1"
        ...........
        ...........
        DB      b+c+d+e+g      ; displays "d"
        DB      a+d+e+f+g      ; displays "E"
        DB      a+e+f+g        ; displays "F"
```


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LCD Control Registers

Table 26–2.LCD Controller Registers

Register	Short Form	Register Type	Address	Initial State
LCD_A control register	LCDACTL	Read/write	090h	Reset with PUC
LCD memory 1	LCDM1	Read/write	091h	Unchanged
LCD memory 2	LCDM2	Read/write	092h	Unchanged
LCD memory 3	LCDM3	Read/write	093h	Unchanged
LCD memory 4	LCDM4	Read/write	094h	Unchanged
LCD memory 5	LCDM5	Read/write	095h	Unchanged
LCD memory 6	LCDM6	Read/write	096h	Unchanged
LCD memory 7	LCDM7	Read/write	097h	Unchanged
LCD memory 8	LCDM8	Read/write	098h	Unchanged
LCD memory 9	LCDM9	Read/write	099h	Unchanged
LCD memory 10	LCDM10	Read/write	09Ah	Unchanged
LCD memory 11	LCDM11	Read/write	09Bh	Unchanged
LCD memory 12	LCDM12	Read/write	09Ch	Unchanged
LCD memory 13	LCDM13	Read/write	09Dh	Unchanged
LCD memory 14	LCDM14	Read/write	09Eh	Unchanged
LCD memory 15	LCDM15	Read/write	09Fh	Unchanged
LCD memory 16	LCDM16	Read/write	0A0h	Unchanged
LCD memory 17	LCDM17	Read/write	0A1h	Unchanged
LCD memory 18	LCDM18	Read/write	0A2h	Unchanged
LCD memory 19	LCDM19	Read/write	0A3h	Unchanged
LCD memory 20	LCDM20	Read/write	0A4h	Unchanged
LCD_A port control 0	LCDAPCTL0	Read/write	0ACh	Reset with PUC
LCD_A port control 1	LCDAPCTL1	Read/write	0ADh	Reset with PUC
LCD_A voltage control 0	LCDAVCTL0	Read/write	0AEh	Reset with PUC
LCD_A voltage control 1	LCDAVCTL1	Read/write	0AFh	Reset with PUC

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LCD_A Control Register

LCDACTL, LCD_A Control Register

7	6	5	4	3	2	1	0
LCDFREQx			LCDMXx		LCDSON	Unused	LCDON
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

LCDFREQx	Bits 7-5	LCD frequency select. These bits select the ACLK divider for the LCD frequency. 000 Divide by 32 001 Divide by 64 010 Divide by 96 011 Divide by 128 100 Divide by 192 101 Divide by 256 110 Divide by 384 111 Divide by 512
LCDMXx	Bits 4-3	LCD mux rate. These bits select the LCD mode. 00 Static 01 2-mux 10 3-mux 11 4-mux
LCDSON	Bit 2	LCD segments on. This bit supports flashing LCD applications by turning off all segment lines, while leaving the LCD timing generator and R33 enabled. 0 All LCD segments are off 1 All LCD segments are enabled and on or off according to their corresponding memory location.
Unused	Bit 1	Unused
LCDON	Bit 0	LCD On. This bit turns on the LCD_A module. 0 LCD_A module off. 1 LCD_A module on.

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LCD_A Port Control Register

LCDAPCTL0, LCD_A Port Control Register 0

7	6	5	4	3	2	1	0
LCDS28	LCDS24	LCDS20	LCDS16	LCDS12	LCDS8	LCDS4	LCDS0†
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

† Segments S0–S3 on the MSP430FG461x devices are disabled from LCD functionality when charge pump is enabled.

LCDS28 Bit 7 LCD segment 28 to 31 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS24 Bit 6 LCD segment 24 to 27 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS20 Bit 5 LCD segment 20 to 23 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS16 Bit 4 LCD segment 16 to 19 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS12 Bit 3 LCD segment 12 to 15 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS8 Bit 2 LCD segment 8 to 11 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS4 Bit 1 LCD segment 4 to 7 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

LCDS0 Bit 0 LCD segment 0 to 3 enable
This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function.
0 Multiplexed pins are port functions.
1 Pins are LCD functions

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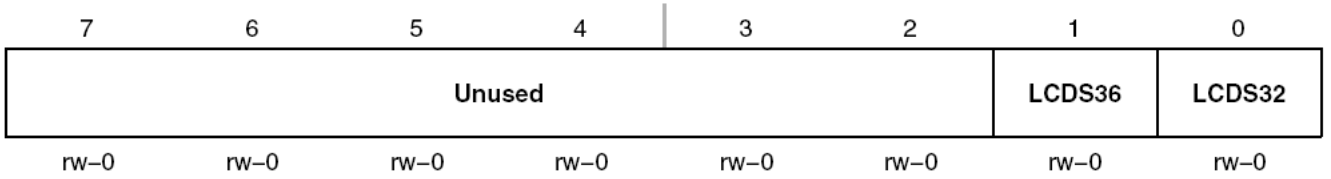
LCD_A Port Control Register (1)

LCDAPCTL1, LCD_A Port Control Register 1



Unused	Bits 7–2	Unused
LCDS36	Bit 1	LCD segment 36 to 39 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions
LCDS32	Bit 0	LCD segment 32 to 35 enable This bit only affects pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0 Multiplexed pins are port functions. 1 Pins are LCD functions

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LCD_A Voltage Control Register (0)

LCDAVCTL0, LCD_A Voltage Control Register 0

7	6	5	4	3	2	1	0
Unused	R03EXT	REXT	VLCDEXT	LCDCPEN	VLCDREFx		LCD2B
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

Unused	Bit 7	Unused
R03EXT	Bit 6	V5 voltage select. This bit selects the external connection for the lowest LCD voltage. R03EXT is ignored if there is no R03 pin available. 0 V5 is AV_{SS} 1 V5 is sourced from the R03 pin
REXT	Bit 5	V2 – V4 voltage select. This bit selects the external connections for voltages V2 – V4. 0 V2 – V4 are generated internally 1 V2 – V4 are sourced externally and the internal bias generator is switched off
VLCDEXT	Bit 4	V_{LCD} source select 0 V_{LCD} is generated internally 1 V_{LCD} is sourced externally
LCDCPEN	Bit 3	Charge pump enable. 0 Charge pump disabled. 1 Charge pump enabled when V_{LCD} is generated internally (VLCDEXT = 0) and VLCDx > 0 or VLCDREFx > 0.
VLCDREFx	Bits 2–1	Charge pump reference select 00 Internal 01 External 10 Reserved 11 Reserved
LCD2B	Bit 0	Bias select. LCD2B is ignored when LCDMx = 00. 0 1/3 bias 1 1/2 bias

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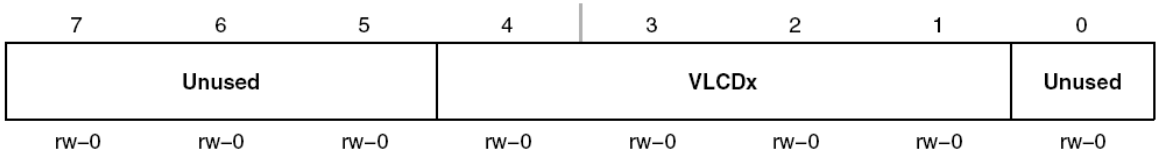
LCD_A Voltage Control Register (1)

LCDAVCTL1, LCD_A Voltage Control Register 1



Unused	Bits 7–5	Unused
VLCDx	Bits 4–1	Charge pump voltage select. LCDCPEN must be 1 for the charge pump to be enabled. AV_{CC} is used for V_{LCD} when VLCDx = 0000 and VREFx = 00 and VLCDEXT = 0. 0000 Charge pump disabled 0001 V_{LCD} = 2.60 V 0010 V_{LCD} = 2.66 V 0011 V_{LCD} = 2.72 V 0100 V_{LCD} = 2.78 V 0101 V_{LCD} = 2.84 V 0110 V_{LCD} = 2.90 V 0111 V_{LCD} = 2.96 V 1000 V_{LCD} = 3.02 V 1001 V_{LCD} = 3.08 V 1010 V_{LCD} = 3.14 V 1011 V_{LCD} = 3.20 V 1100 V_{LCD} = 3.26 V 1101 V_{LCD} = 3.32 V 1110 V_{LCD} = 3.38 V 1111 V_{LCD} = 3.44 V
Unused	Bit 0	Unused

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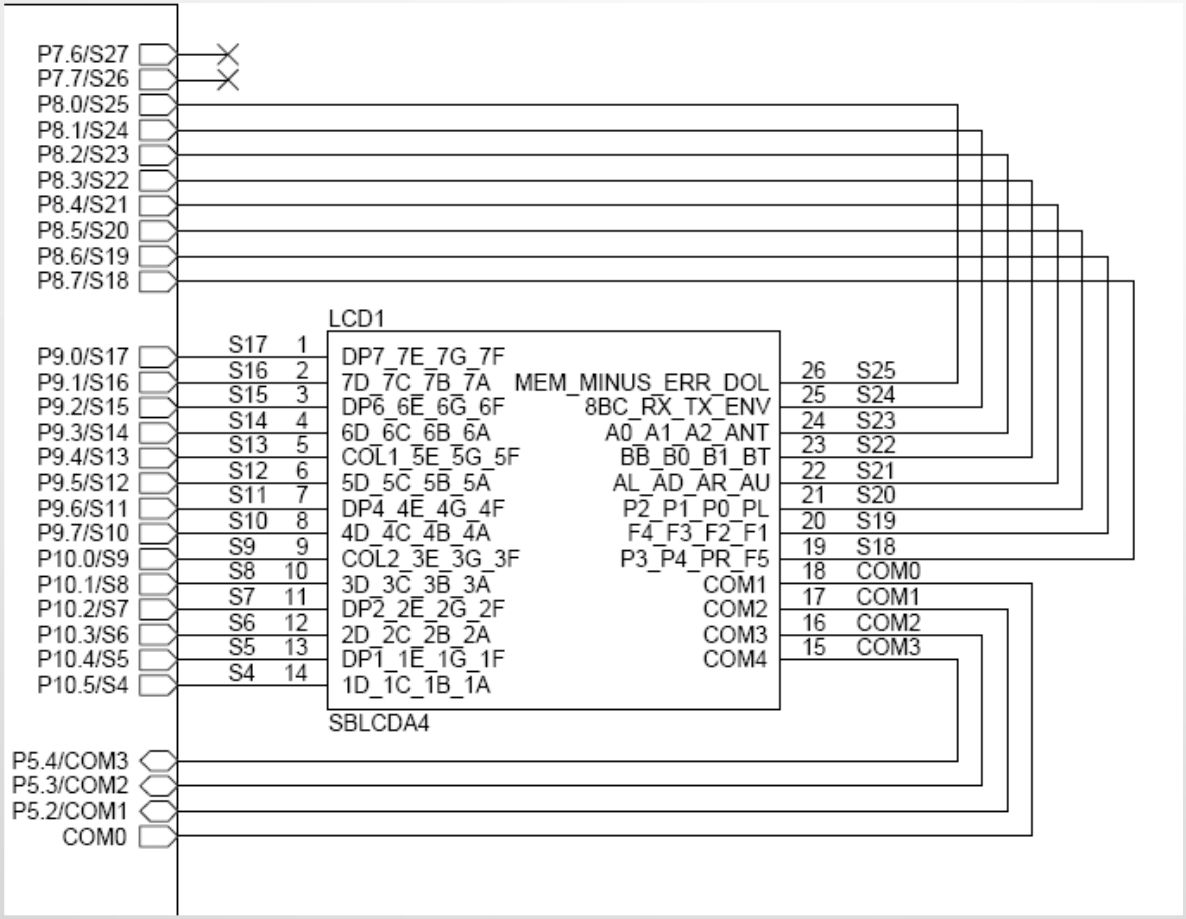
DRFG4618 LCD Interface



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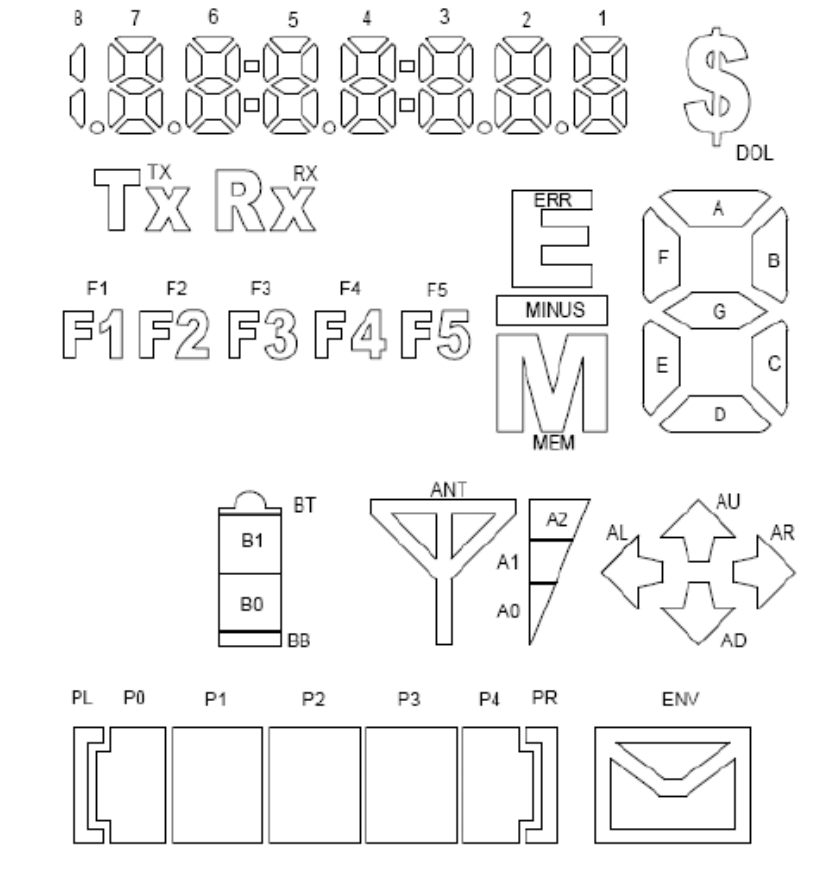
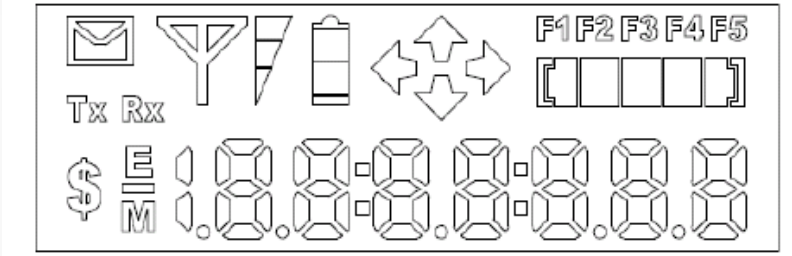
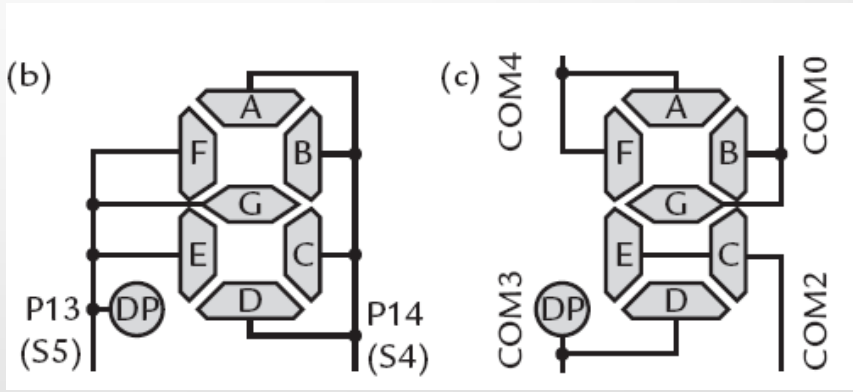
Softbaugh LCD SBLCDA4: Segment Description

SBLCDA4 Display







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Mapping SBCDA4 segments to MSP430 pins (TI Experimenter board)

			COM:	3	2	1	0	3	2	1	0		
display memory	MSP430 pin	LCD pin		S_{n+1}				S_n				LCD pin	MSP430 pin
LCDM13	S25	P26		MEM	MIN	ERR	DOL	8BC	RX	TX	ENV	P25	S24
LCDM12	S23	P24		A0	A1	A2	ANT	BB	B0	B1	BT	P23	S22
⋮	⋮	⋮										⋮	⋮
LCDM4	S7	P11		DP2	2E	2G	2F	2D	2C	2B	2A	P12	S6
LCDM3	S5	P13		DP1	1E	1G	1F	1D	1C	1B	1A	P14	S4
			Bit:	7	6	5	4	3	2	1	0		