

# CPE 323: MSP430 Digital I/O

Aleksandar Milenkovic

Electrical and Computer Engineering  
The University of Alabama in Huntsville

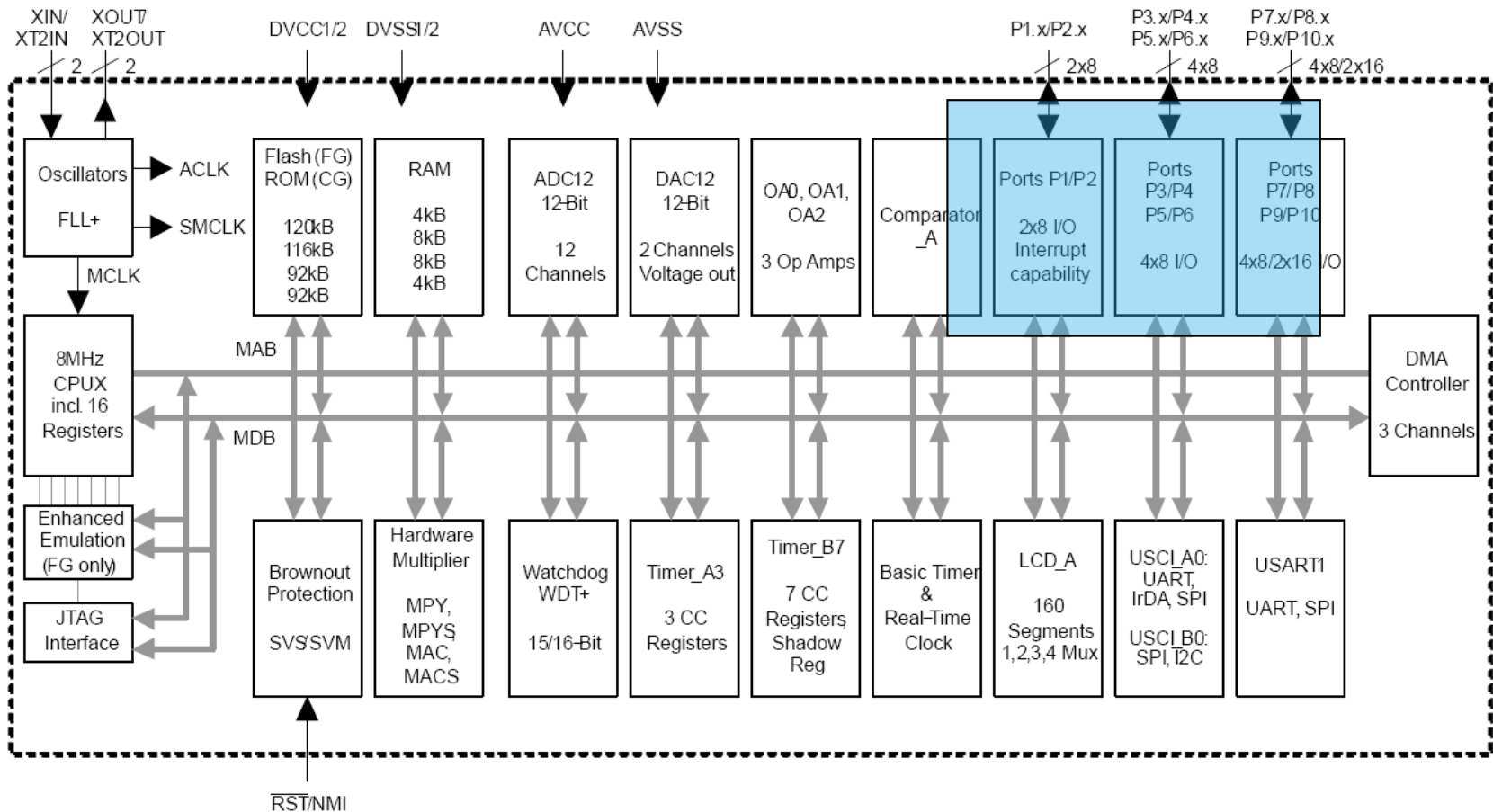
[milenka@ece.uah.edu](mailto:milenka@ece.uah.edu)

<http://www.ece.uah.edu/~milenka>

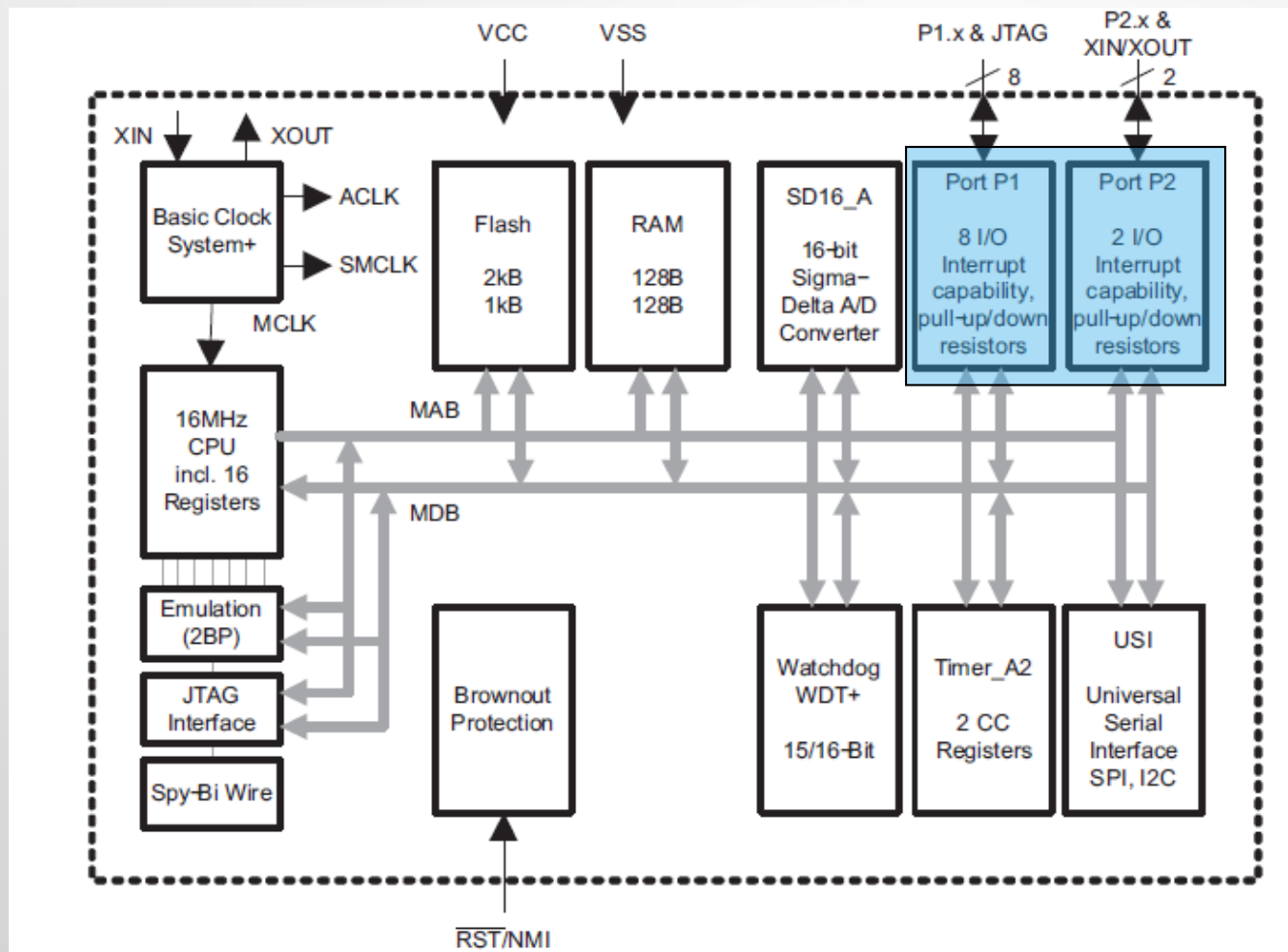
# Outline

- System View
- Digital I/O
- Address Mapping
- Port Operations
- Schematics
- Configuration

# Functional Block Diagram of MSP430xG461x



# Functional Block Diagram of MSP430xF20x3



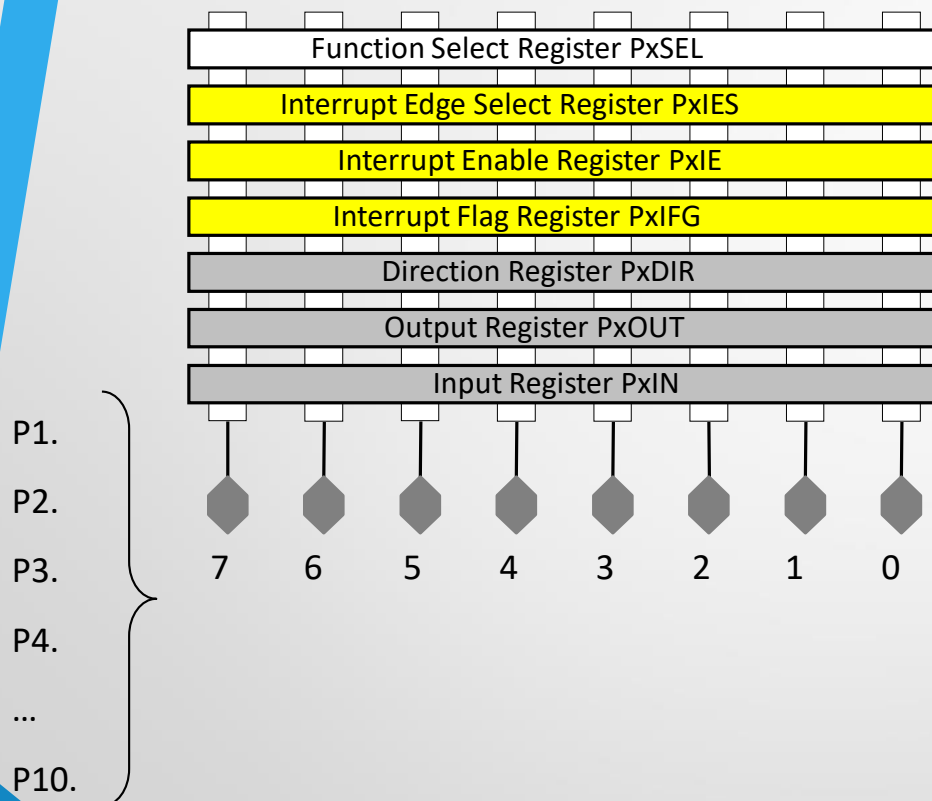
# Digital Input, Output

- Digital inputs – they are either on or off
  - Inputs from humans or sensors
  - E.g., switches, sensors (e.g., door is locked, button is pressed, ...)
- Digital outputs – set them on or off
  - Light-emitting diodes (LEDs), seven segment displays, liquid-crystal displays (LCDs)
  - MSP430 can supply these directly if they work from the same voltage and draw a sufficiently small current
- Digital input/output ports (P1 – Pn),  $n=2 \dots 10$ 
  - Almost all pins can be used either for digital I/O or for other (special) functions
  - Their operation must be configured on start up

# Digital Input, Output (cont'd)

- Ports P1 and P2 have interrupt capability
- Each interrupt for the P1 and P2 input lines can be individually enabled and configured to provide an interrupt on a rising edge or falling edge of an input signal
- The digital I/O features include:
  - Independently programmable individual I/Os
  - Any combination of input or output
  - Individually configurable P1 and P2 interrupts
  - Independent input and output data registers
- The digital I/O is configured with user software

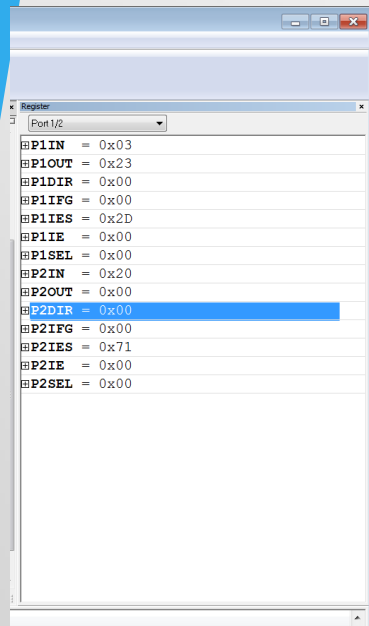
# Parallel Ports



Port1 Port2	Port3 ... Port10
yes	yes
yes	no
yes	no
yes	no
yes	yes
yes	yes
yes	yes

# IAR View of Digital I/O Ports

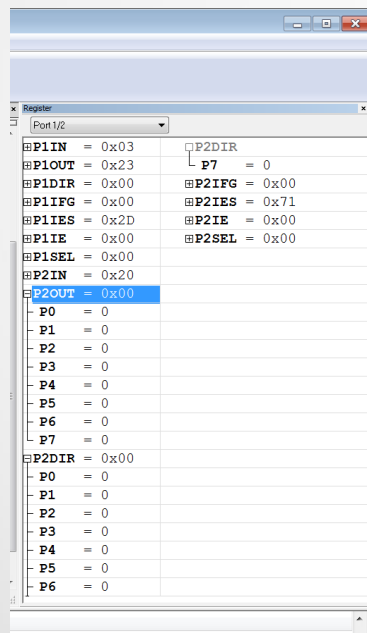
P<sub>1</sub>, P<sub>2</sub>



```

Register
Port 1/2
#P1IN = 0x03
#P1OUT = 0x23
#P1DIR = 0x00
#P1IFG = 0x00
#P1IES = 0x2D
#P1IE = 0x00
#P1SEL = 0x00
#P2IN = 0x20
#P2OUT = 0x00
#P2DIR = 0x00
#P2IFG = 0x00
#P2IES = 0x71
#P2IE = 0x00
#P2SEL = 0x00
  
```

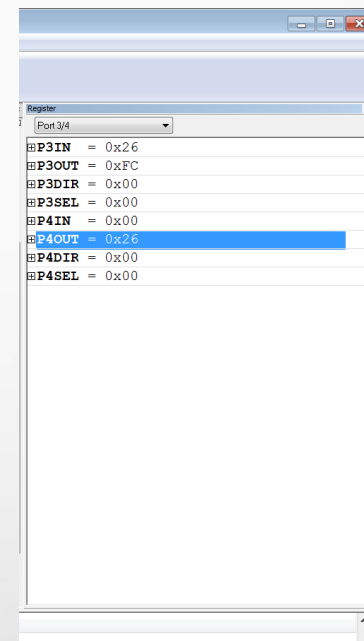
P<sub>1</sub>, P<sub>2</sub>,  
Expanded view



```

Register
Port 1/2
#P1IN = 0x03
#P1OUT = 0x23
#P1DIR = 0x00
#P1IFG = 0x00
#P1IES = 0x2D
#P1IE = 0x00
#P1SEL = 0x00
#P2IN = 0x20
#P2OUT = 0x00
#P2DIR = 0x00
P0 = 0
P1 = 0
P2 = 0
P3 = 0
P4 = 0
P5 = 0
P6 = 0
P7 = 0
#P2DIR = 0x00
P0 = 0
P1 = 0
P2 = 0
P3 = 0
P4 = 0
P5 = 0
P6 = 0
  
```

P<sub>3</sub>, P<sub>4</sub>,  
Expanded view



```

Register
Port 3/4
#P3IN = 0x26
#P3OUT = 0xFC
#P3DIR = 0x00
#P3SEL = 0x00
#P4IN = 0x00
#P4OUT = 0x26
#P4DIR = 0x00
#P4SEL = 0x00
  
```



# MSP430FG4618 Port Address Mapping

- Notice addresses of P9.IN and P10.IN, P9.OUT and P10.OUT
  - Other pairs of register too
- What are implications?

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P10	Port P10 selection	P10SEL	00Fh
	Port P10 direction	P10DIR	00Dh
	Port P10 output	P10OUT	00Bh
	Port P10 input	P10IN	009h
Port P9	Port P9 selection	P9SEL	00Eh
	Port P9 direction	P9DIR	00Ch
	Port P9 output	P9OUT	00Ah
	Port P9 input	P9IN	008h
Port P8	Port P8 selection	P8SEL	03Fh
	Port P8 direction	P8DIR	03Dh
	Port P8 output	P8OUT	03Bh
	Port P8 input	P8IN	039h
Port P7	Port P7 selection	P7SEL	03Eh
	Port P7 direction	P7DIR	03Ch
	Port P7 output	P7OUT	03Ah
	Port P7 input	P7IN	038h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h

# MSP430F2013 Port Address Mapping

- There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2
  - Each I/O has an individually programmable pullup/pulldown resistor

Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h

# Digital I/O Registers: Operation

- Input Register PnIN

- Each bit in each PnIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.
  - Bit = 0: The input is low
  - Bit = 1: The input is high

Do not write to PxIN. It will result in increased current consumption

- Output Registers PnOUT

- Each bit in each PnOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function and output direction.
  - Bit = 0: The output is low
  - Bit = 1: The output is high

# Digital I/O Registers: Operation

- Direction Registers PnDIR
  - Bit = 0: The port pin is switched to input direction
  - Bit = 1: The port pin is switched to output direction
- Function Select Registers PnSEL
  - Port pins are often multiplexed with other peripheral module functions.
    - Bit = 0: I/O Function is selected for the pin
    - Bit = 1: Peripheral module function is selected for the pin

# Digital I/O Registers: Operation

- Interrupt Flag Registers P1IFG, P2IFG (only for P1 and P2)
  - Bit = 0: No interrupt is pending
  - Bit = 1: An interrupt is pending
- Only transitions, not static levels, cause interrupts
- Interrupt Edge Select Registers P1IES, P2IES
  - Each PnIES bit selects the interrupt edge for the corresponding I/O pin (n=1, 2).
    - Bit = 0: The PnIFGx flag is set with a low-to-high transition
    - Bit = 1: The PnIFGx flag is set with a high-to-low transition

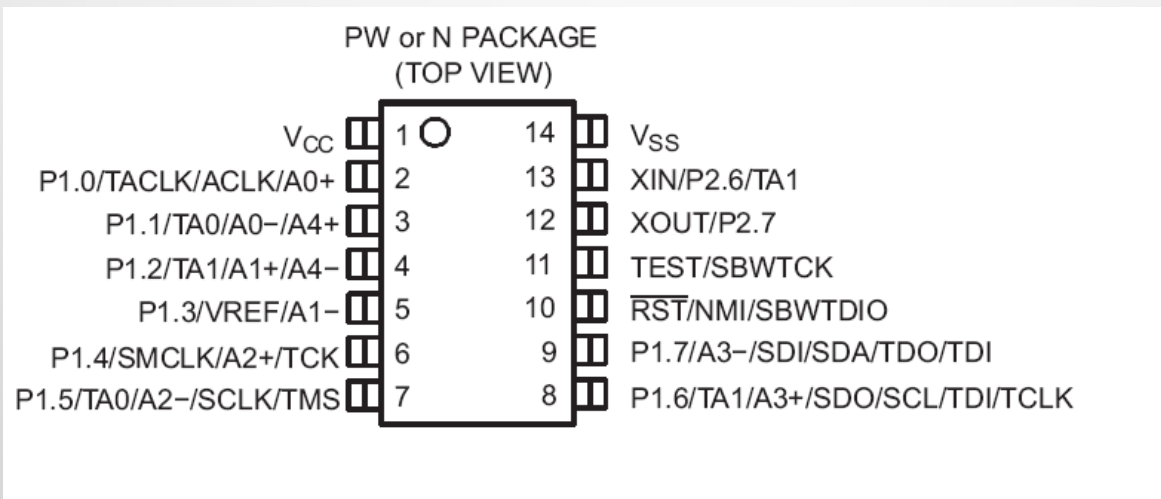
# Digital I/O Registers: Operation (Specific for MSP430F2xxx)

- Pullup/Pulldown Resistor Enable Registers PxREN
  - Each bit in each PxREN register enables or disables the pullup/pulldown resistor of the corresponding I/O pin
  - The corresponding bit in the PxOUT register selects if the pin is pulled up or pulled down
    - Bit = 0: Pullup/pulldown resistor disabled
    - Bit = 1: Pullup/pulldown resistor enabled

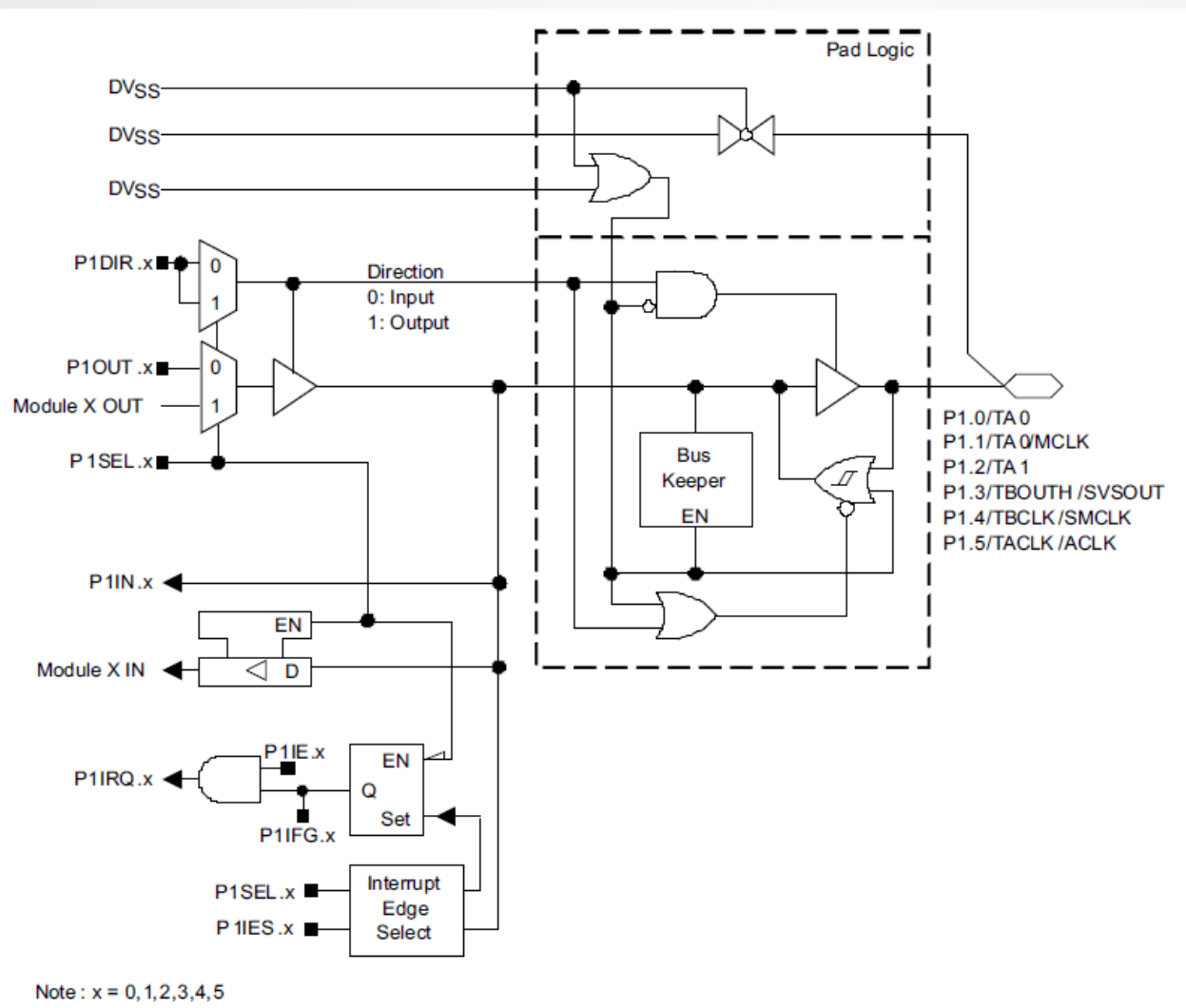
# Digital I/O Registers: Operation (Specific for MSP430F2xxx)

- Two select registers PxSEL and PxSEL2

PxSEL2	PxSEL	Pin Function
0	0	I/O function is selected.
0	1	Primary peripheral module function is selected.
1	0	Reserved. See device-specific data sheet.
1	1	Secondary peripheral module function is selected.

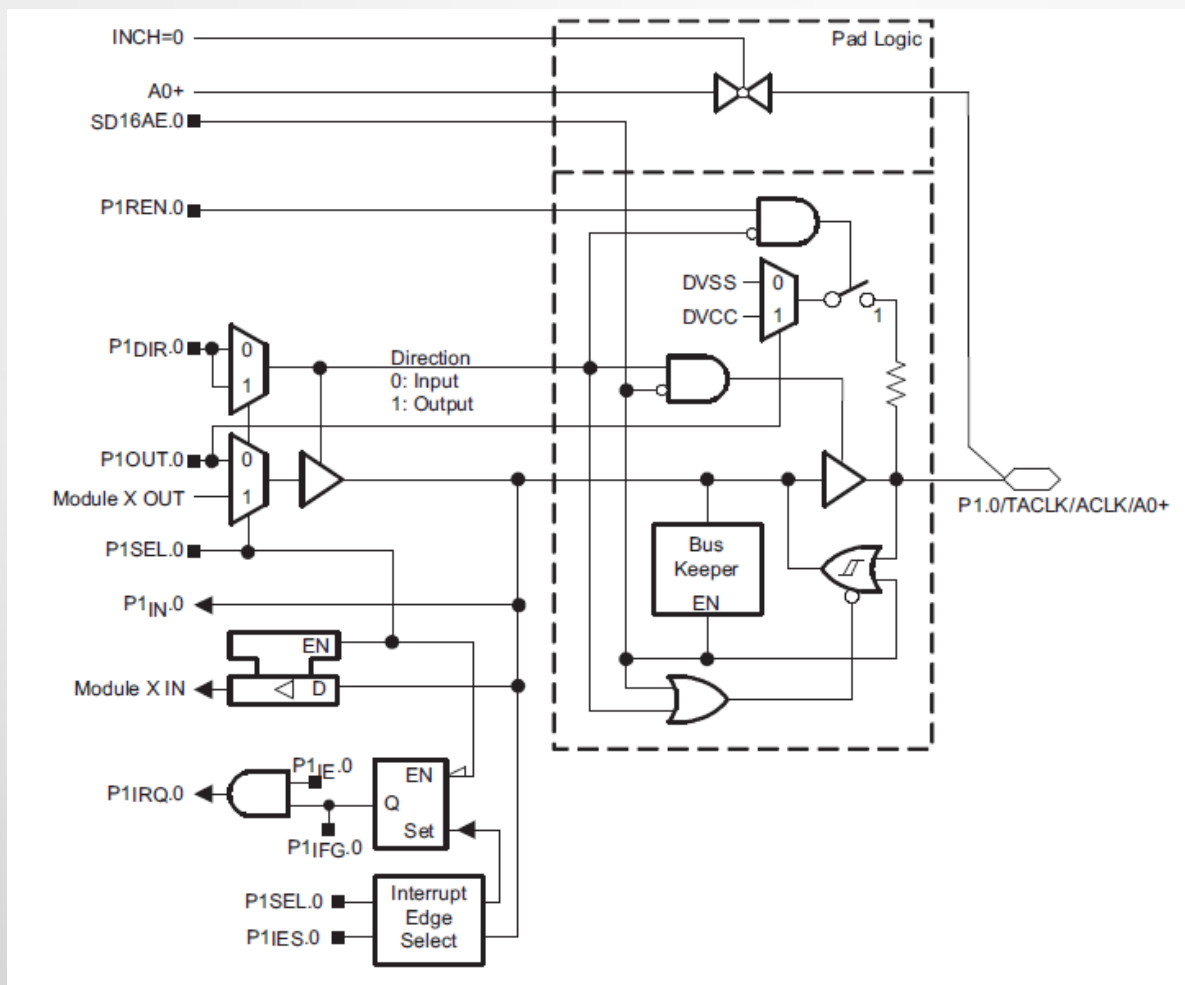


# MSP430FG4618 P1.0-5 Schematic





# MSP430F20x3 Port P1 Schematic



# Configuring Unused Pins

- Unused pins must never be left unconnected in their default state as inputs
  - Floating (unconnected) input – both pull-up and pull-down may be causing shoot-through current => deplete your power source
- What should you do?
  - Wire unused pins externally to  $V_{GND}$  or  $V_{DD}$  and configure them as inputs (Warning: if you accidentally configure them as outputs you may damage the chip)
  - Leave the pins unconnected externally, but connect them internally to  $V_{GND}$  or  $V_{DD}$  (applicable only to MSP430F2xx devices)
  - Leave the pins unconnected and configure them as outputs (Warning: do not short circuit them with the probe)