CPE 323
MODULE 07
MSP430 System Architecture

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Overview

This module discusses a system view of MSP430 - a system-on-a-chip that integrates processor core, flash memory, RAM memory, hardware accelerators, and I/O peripherals through a shared system bus. You will learn about individual components and how they interface external world via pins tied to parallel ports.

Objectives

Upon completion of this module learners will be able to:

- *Recognize organization of MSP430 SoCs with all individual I/O interfaces and their purpose*
- *Interpret a generic view of an I/O peripheral device with control, status, and data registers*
- *Apply principles of software I/O interfacing through polling and ISRs*

Contents

1 Introduction

MSP430 is a system-on-a-chip that integrates an MSP430 processor core, static RAM memory, flash memory, system clock, JTAG/Debug interface, and a number of 8-bit and 16-bit I/O peripherals on a single chip. Figure 1 shows a generic block diagram of a MSP430 family microcontroller. The components are connected through the bus that consists of a memory address bus (MAB) and a memory data bus (MDB). Examples of 8-bit peripherals are parallel ports (P1 – P10), serial communication interfaces (USCI, USI, USART). Note: pair of adjacent 8-bit parallel ports can be viewed as a single 16-bit parallel port. Examples of 16-bit peripherals are watchdog timer (WDT), timers (TimerA, TimerB, real-time clock), analog-to-digital (ADC12) and digital-to-analog (DAC12) converters, direct memory access controller (DMA), and flash memory controller (FTC).

The MSP430 family includes several hundred different microcontrollers. They differ in size of RAM and flash memory, type and number of peripherals, clock speeds, the number of pins, and type of packaging. This way, customers with diverse needs and requirements can find a device that suites their needs and price points.

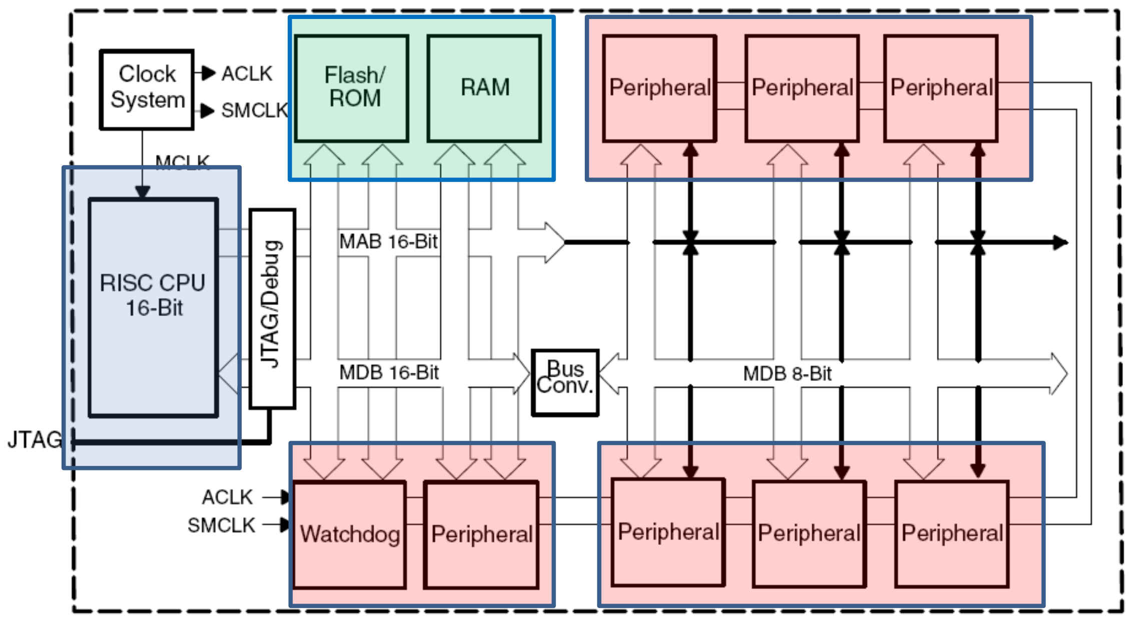

Figure 1. General block diagram of an MSP430 family microcontroller.

Here we will give a brief description of major components found in MSP430 SoCs.

- CPU (Central Processing Unit / Processor) – executes programs. There are several variants of cores, the baseline 16-bit MSP430, and several versions of extended architecture that supports 20-bit general-purpose registers.
- SRAM (Static RAM) – volatile memory is used for program stack and heap; it is fast and energy-efficient, but it loses its content when the power is turned off.
- Flash/FRAM – non-volatile memory for holding programs and data; the non-volatile memories retain their content even when power is turned off;

- Clock subsystem – generates clocks used by the rest of the system. Usually 3 clocks are provided: Main Clock – MCLK used by the CPU, memories, and selected peripherals, Sub-Main Clock – SMCLK used by peripherals, and Auxiliary Clock – ACLK used by peripherals. There are several types of clock subsystems in MSP430 family differing in clock speeds and inner organization. They all expose clock control to software – i.e., clocks can be adjusted in runtime without stopping the processor or even they can be turned off when not needed to save energy which is important in battery-operated devices.
- JTAG/Debug – allows for loading programs into non-volatile memory and enables debugging. The debug interface allows for controlled program execution through JTAG, specifically we can execute a single instruction at a time or a sequence of instructions until a breakpoint in the program is reached. When the program execution stops, we can inspect the content of registers and memory locations through the JTAG. This is critical feature to help us find bugs in our programs.
- Timers – enable measuring time, generating pulse-width modulated signals, and capturing timestamps when certain events in hardware occur.
- Serial communication interfaces – implement various serial communication protocols, such as UART, SPI, I^2C, CAN, USB, and others. These protocols enable our MSP430-based system to communicate with outside world.
- Parallel ports – implement standard digital inputs/outputs or special-purpose signals (e.g., data transmit lines for communication protocols, or analog inputs for ADC12).
- Analog-to-digital converters – convert analog inputs (voltages) into digital counterparts.
- Digital-to-analog converters – convert digital values into analog signals (voltages).
- Direct memory access controllers – carry out data transfer operations without processor intervention and thus speed up data transfers between input peripherals and memory, input and output peripherals, between memory and output peripherals, and between two buffers in memory.

In the rest of the course, we will learn more about many of these peripheral devices, including their functionality, programmers view (format and type of registers visible to software developers), and hardware organization.

2 Examples of MSP430 microcontrollers

Figure 2 shows a block diagram of MSP430FG46{16, 17, 18, 19} chips. The CPU core features an extended architecture with 20-bit general-purpose registers. Thus the size of the flash memory ranges between 92 KB and 120 KB, and the range of RAM is either 4 KB or 8 KB. MSP430FG4618 chip is the heart of the MSP430 Experimenter board shown in Figure 3 and it has 116 KB flash and 8 KB RAM memory. It has 10 parallel ports (P1-P10) that provide interface to the rest of the world through port pins (P1.0 – P1.7, P2.0 – P2.7, … P10.0 – P10.7). The clock module is FLL+ providing 3 clocks running at up to 8 MHz clock frequency. The analog complex includes an AD converter, ADC12, a DA converter, DAC12, 3 operational amplifiers (OA1, OA2, OA3), and a comparator (COMP_A). The timer complex includes the watchdog timer (WDT), TimerA3, TimerB7, and a Basic Timer and Real-time Clock. Two peripherals supporting serial communication are USCI and USART1. In addition to these, 4xx family includes an LCD controller (LCD_A in this case) for interfacing liquid crystal displays with up to 160 different segments. This chip also includes a hardware multiplier, a hardware accelerator supporting unsigned and signed integer multiplication and multiply-and-accumulate operations.

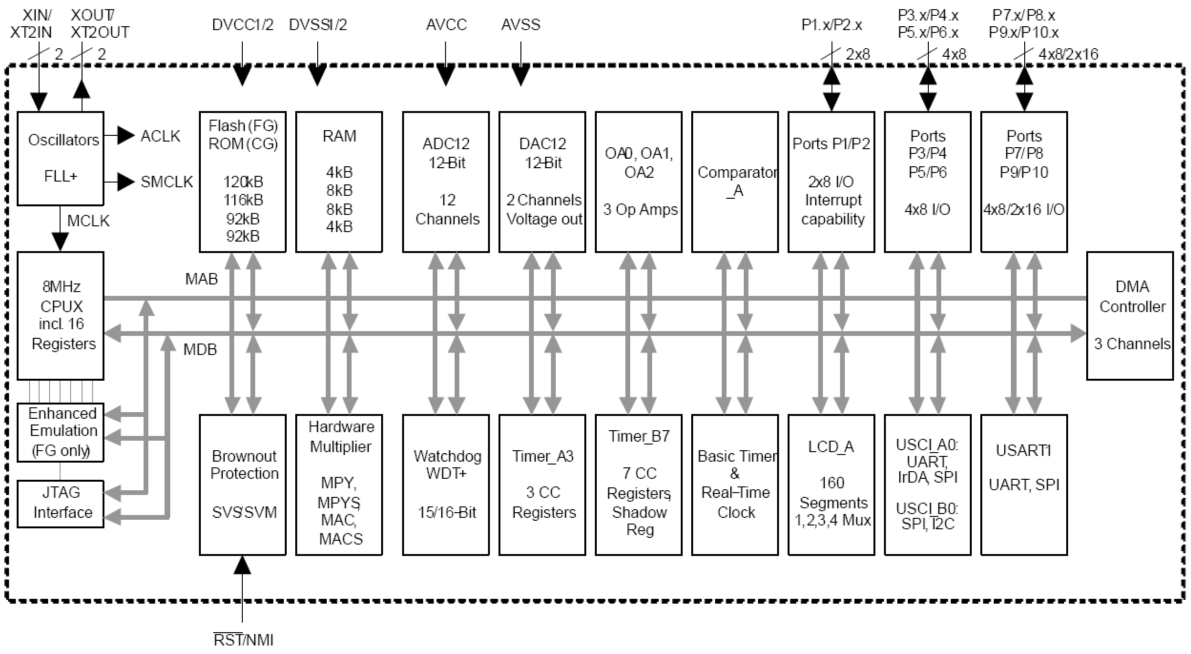
XIN/ XT2IN
XOUT/ XT2OUT
2
2
DVCC1/2
DVSS1/2
AVCC
AVSS
P1.x/P2.x
2x8
P3.x/P4.x P5.x/P6.x
4x8
P7.x/P8.x P9.x/P10.x
4x8/2x16
Oscillators FLL+
ACLK
SMCLK
MCLK
Flash (FG) ROM (CG) 120kB 116kB 92kB 92kB
RAM 4kB 8kB 8kB 4kB
ADC12 12-Bit 12 Channels
DAC12 12-Bit 2 Channels Voltage out
OA0, OA1, OA2 3 Op Amps
Comparator _A
Ports P1/P2 2x8 I/O Interrupt capability
Ports P3/P4 P5/P6 4x8 I/O
Ports P7/P8 P9/P10 4x8/2x16 I/O
8MHz CPUX incl. 16 Registers
MAB
MDB
DMA Controller 3 Channels
Enhanced Emulation (FG only)
JTAG Interface
Brownout Protection SVS/SVM
Hardware Multiplier MPY, MPYS, MAC, MACS
Watchdog WDT+ 15/16-Bit
Timer_A3 3 CC Registers
Timer_B7 7 CC Registers, Shadow Reg
Basic Timer & Real-Time Clock
LCD_A 160 Segments 1,2,3,4 Mux
USCI_A0: UART, IrDA, SPI USCI_B0: SPI, I2C
USART1 UART, SPI
RST/NMI

Figure 2. Block diagram of MSP430FG4616/MSP430FG4617/MSP430FG4618/MSP430FG4619.

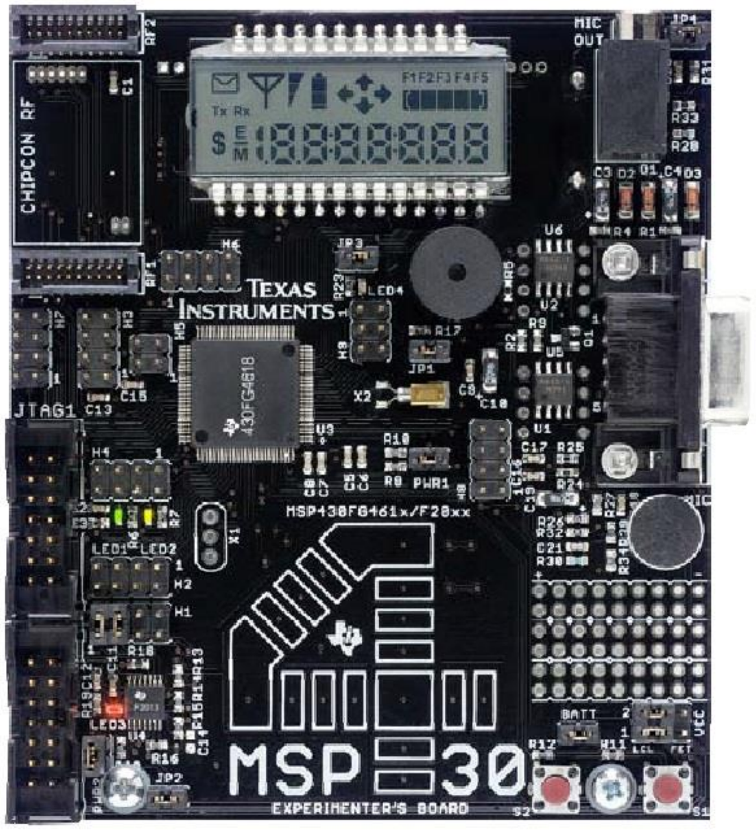

Figure 3. MSP430's Experimenter Board.

Figure 4 shows a functional block diagram of MSP430F55{21, 25, 25, 29} chips. The CPU core features an extended architecture, version 2. The size of the flash memory ranges between 32 KB and 128 KB, and the size of RAM memory is 4 KB, 6 KB or 8 KB, plus 2 KB of RAM reserved for a USB controller. MSP430F5529 chip is the heart of the MSP430 Launchpad shown in Figure 5 and it has 128 KB flash and 8 KB RAM memory. It has 8 parallel ports (P1-P8) that provide interface to the rest of the world through port pins (P1.0 – P1.7, P2.0 – P2.7, … P8.0 – P8.7). The clock module is Unified Clock System providing 3 clocks running at up to 25 MHz. The analog complex includes an AD converter, ADC12_A and a comparator (COMP_B). The timer complex includes three TA timers (TA0, TA1, and TA2) and one TimerB (TB0), and a Real-time Clock. Serial communication interfaces are USCI0 and USCI1. This chip also includes a hardware multiplier, MPY32, a hardware accelerator supporting unsigned and signed integer multiplication and multiply-and-accumulate operations. The SYS module includes a watchdog and Port Map Control (P4).

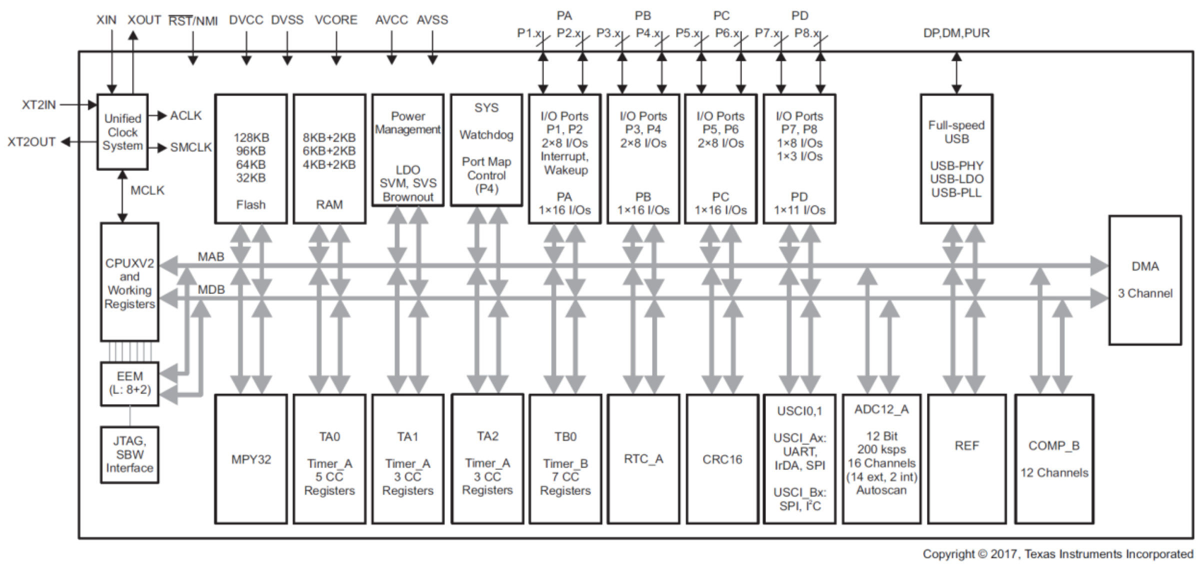
XIN
XOUT
RST/NMI
DVCC
DVSS
VCORE
AVCC
AVSS
PA
PB
PC
PD
P1.x
P2.x
P3.x
P4.x
P5.x
P6.x
P7.x
P8.x
DP,DM,PUR
XT2IN
XT2OUT
Unified Clock System
ACLK
SMCLK
MCLK
128KB 96KB 64KB 32KB Flash
8KB+2KB 6KB+2KB 4KB+2KB RAM
Power Management LDO SVM, SVS Brownout
SYS Watchdog Port Map Control (P4)
I/O Ports P1, P2 2×8 I/Os Interrupt, Wakeup PA 1×16 I/Os
I/O Ports P3, P4 2×8 I/Os PB 1×16 I/Os
I/O Ports P5, P6 2×8 I/Os PC 1×16 I/Os
I/O Ports P7, P8 1×8 I/Os 1×3 I/Os PD 1×11 I/Os
Full-speed USB USB-PHY USB-LDO USB-PLL
CPUXV2 and Working Registers
MAB
MDB
DMA 3 Channel
EEM (L: 8+2)
JTAG, SBW Interface
MPY32
TA0 Timer_A 5 CC Registers
TA1 Timer_A 3 CC Registers
TA2 Timer_A 3 CC Registers
TB0 Timer_B 7 CC Registers
RTC_A
CRC16
USCI0,1 USCI_Ax: UART, IrDA, SPI USCI_Bx: SPI, I²C
ADC12_A 12 Bit 200 ksps 16 Channels (14 ext, 2 int) Autoscan
REF
COMP_B 12 Channels
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Figure 4. Block diagram of MSP430F55z{21, 25, 27, 29}.

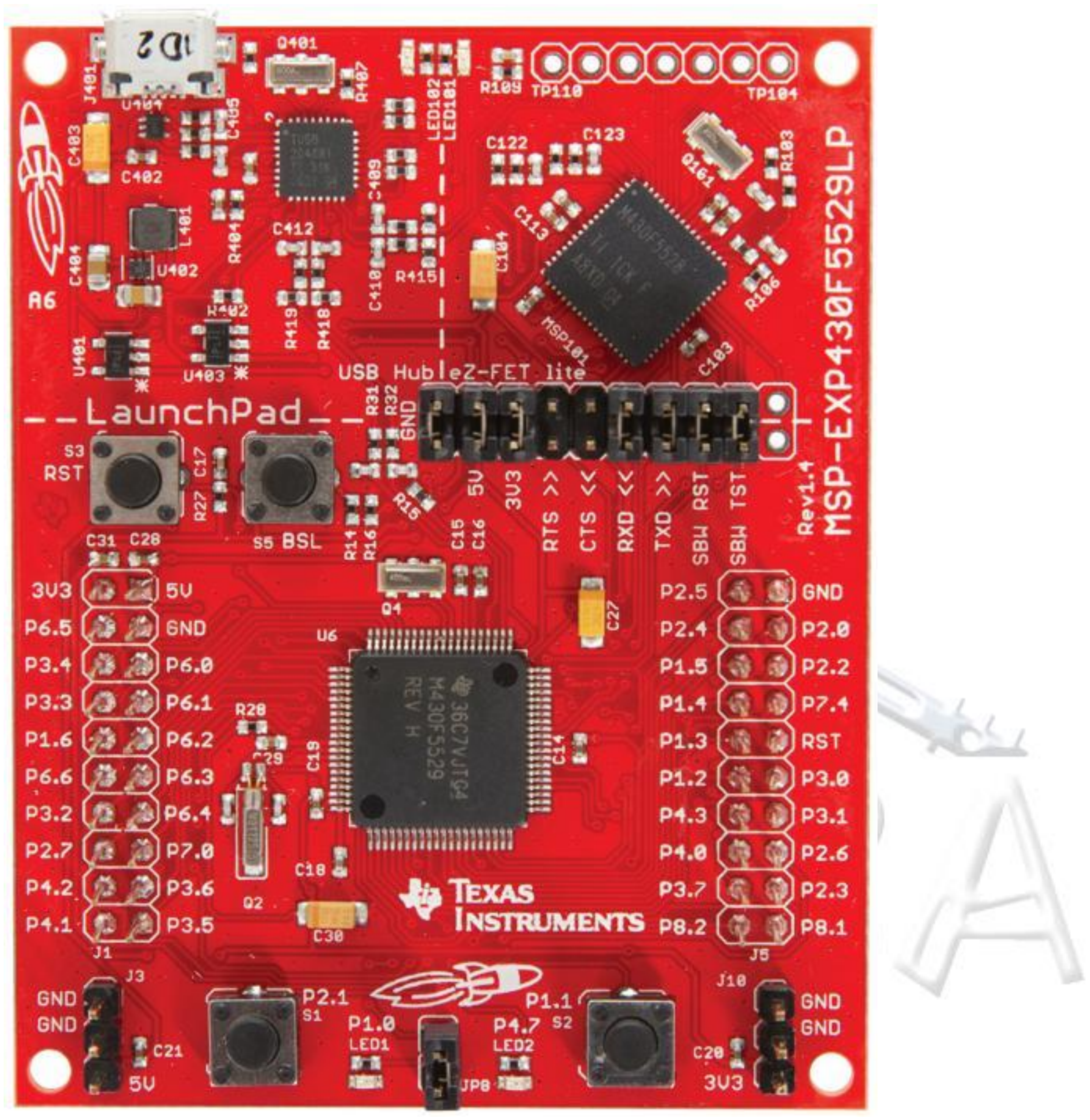


Figure 5. EXP430F5529LP Launchpad Board.

3 Pin Diagrams

Understanding pin diagram is necessary to be able to read board schematics. Figure 6 shows a pin diagram of the MSP430FG4618 that comes in a 100-pin PZ or plastic quad flatpack package. PZ is TI's name for LQFP – low-profile quad flat package. Note: A low-profile quad flat package is a surface mount integrated circuit package format with component leads extending from each of the four sides. Pins are numbered counter-clockwise from the index dot. Spacing between pins can vary; common spacings are 0.4, 0.5, 0.65 and 0.80 mm intervals.

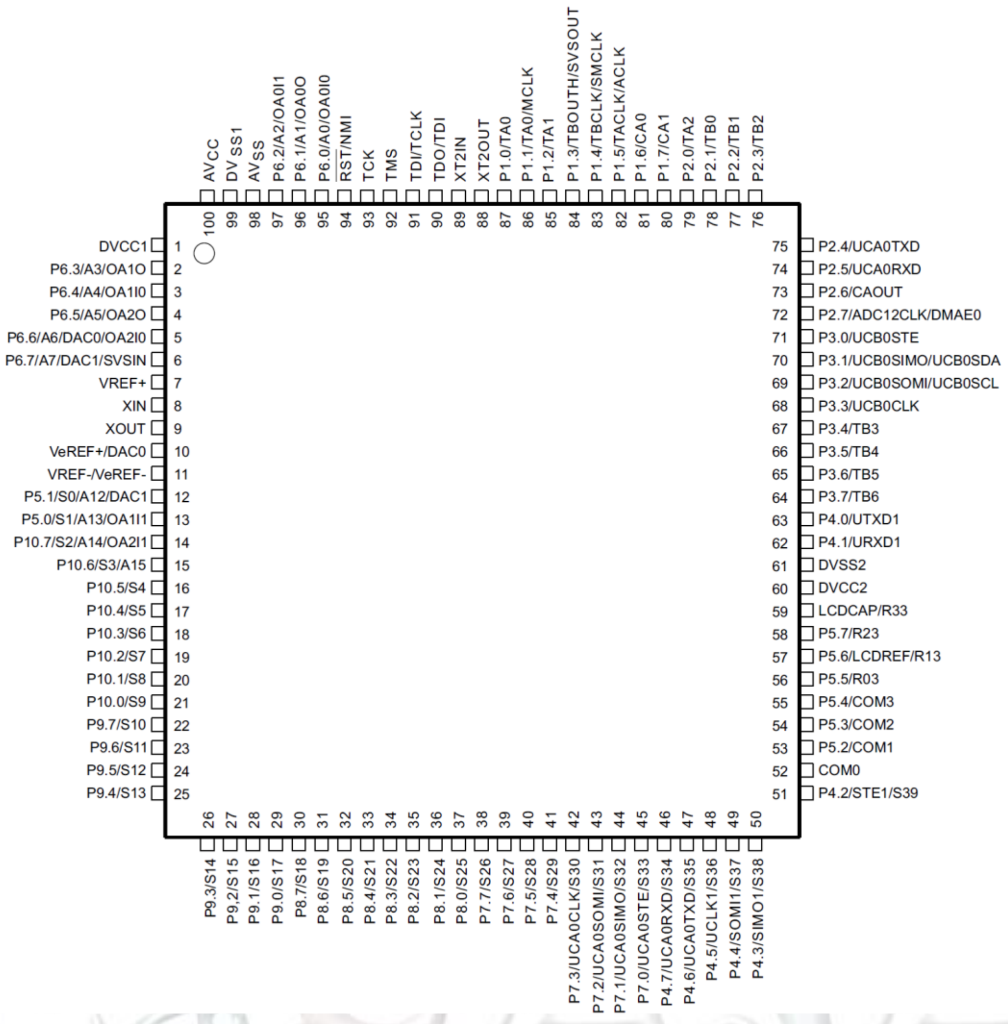


Figure 6. Pin Diagram of MSP430FG4618 Chip.

Each side has 25 pins, where PIN_1 is DVCC1 (digital supply voltage, positive terminal) and PIN_100 is ACC1 (analog supply voltage, positive terminal that powers oscillator, SVS module, and COMP_A). In addition to ground pins (DV_{SS1}, AV_{SS1}, DV_{SS2}), JTAG pins (TMS, TCK, TDI/TCLK, TDO/TDI), and clock related pins (XT2IN, XT2OUT, XIN, XOUT), majority of other pins are multiplexed and can connected to parallel ports P1-P10. When connected to parallel ports, they act as digital input/output pins, configurable through corresponding PxDIR registers. However, they can be configured to act as special-function pins, connected to particular peripheral devices. For example, in digital mode (P1SEL.BIT0 is '0') PIN_87 is connected to P1.0 (port 1, pin 0) that is further connected to P1OUT.BIT0 if P1DIR.BIT0 is '1' (digital output) or to P1IN.BIT0 if P1DIR.BIT0 is '0' (digital input). However, if a special mode of operation is selected, i.e., P1SEL.BIT0 is '1', then the PIN_87 connects to the output or input of the TA0 (Timer A, capture&compare block 0 signal). Practically every pin has dual functionality – it connects to a parallel port bit in digital I/O mode, or serves as a special signal tied to a certain peripheral. This is done to reduce the number of pins and the size of the chip (and thus its cost). There is a saying in semiconductor industry "If transistors are made of silver, pins are made of gold," indicating how each aspect impacts the cost of the chip. A fun fact is that silver and gold are indeed used in manufacturing of transistors and pins, respectively.

The information about individual pins and their function can be found in corresponding device-specific technical document –slas508j in case of MSP430FG4618.

Figure 7 shows a pin diagram for MSP430F5529 device that comes in a 80-pin PN package (PN is a TI's name for 80-pin low profile quad flat package) discussed above. Each side has 20 pins. Similarly to MSP430FG4618, majority of pins are multiplexed between parallel ports (P1 – P8) and special functions. You will notice that some pins are triple-multiplexed (e.g., PIN_44 to PIN_48). A detailed description of each pin function for this device can be found in the TI's slas590N document.

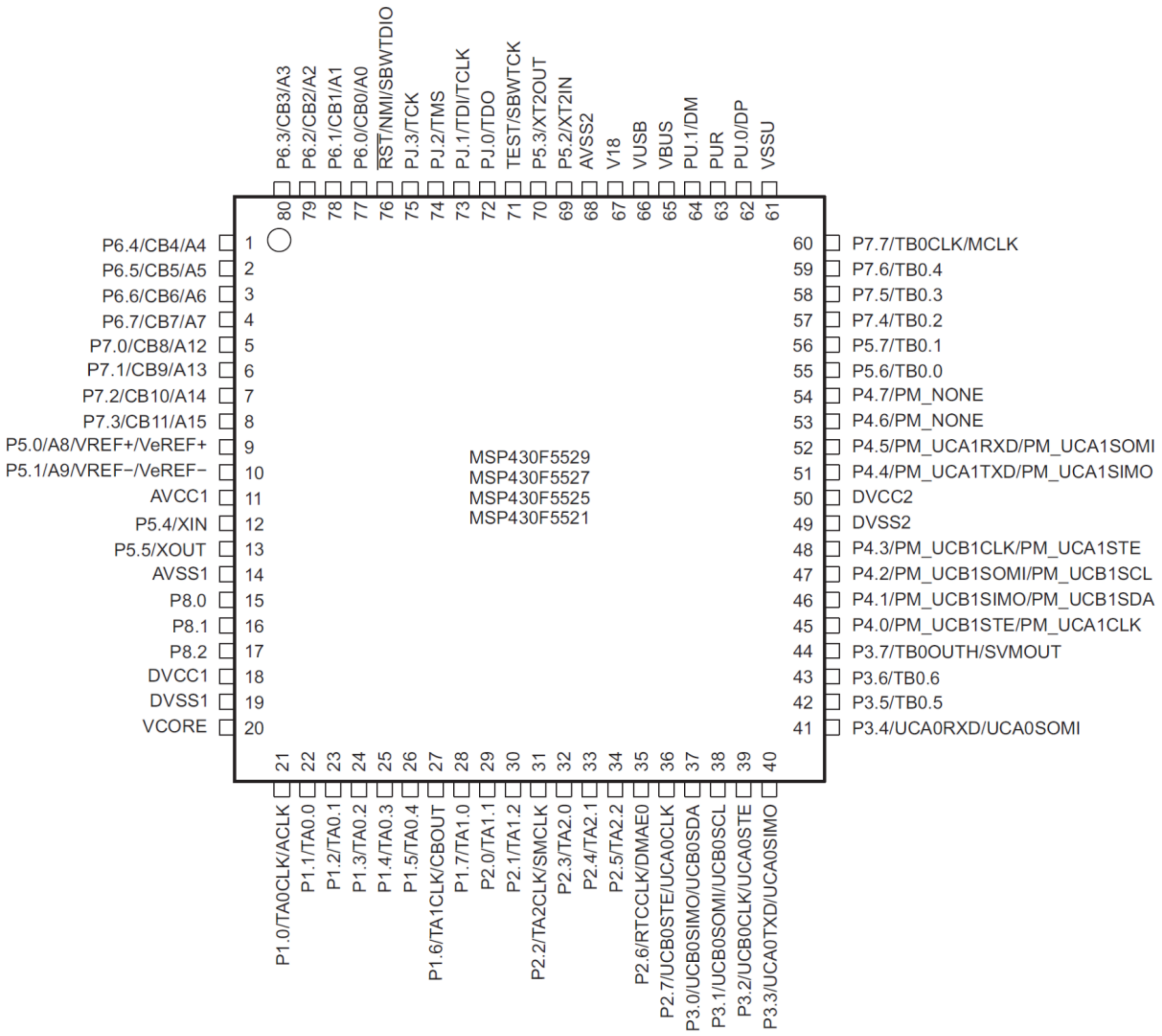


Figure 7. Pin Diagram of MSP430F5529 Chip.

4 Getting Started with TI Experimenter's Board

The TI Experimenter's Board includes two microcontrollers (MSP430F4168 and MSP430F2013), two JTAGs, 2 buttons, several LEDs, a capacitive touch pad, a microphone, a buzzer, an LCD, socket for a wireless interface, analog output, and a RS232 serial port. Figure 8 shows a photo of the TI Experimenter's Board and the corresponding block diagram that illustrates major components. **IMPORTANT Note: make sure that you use JTAG1 when working with FG4618 and JTAG2 when working with G2013.**

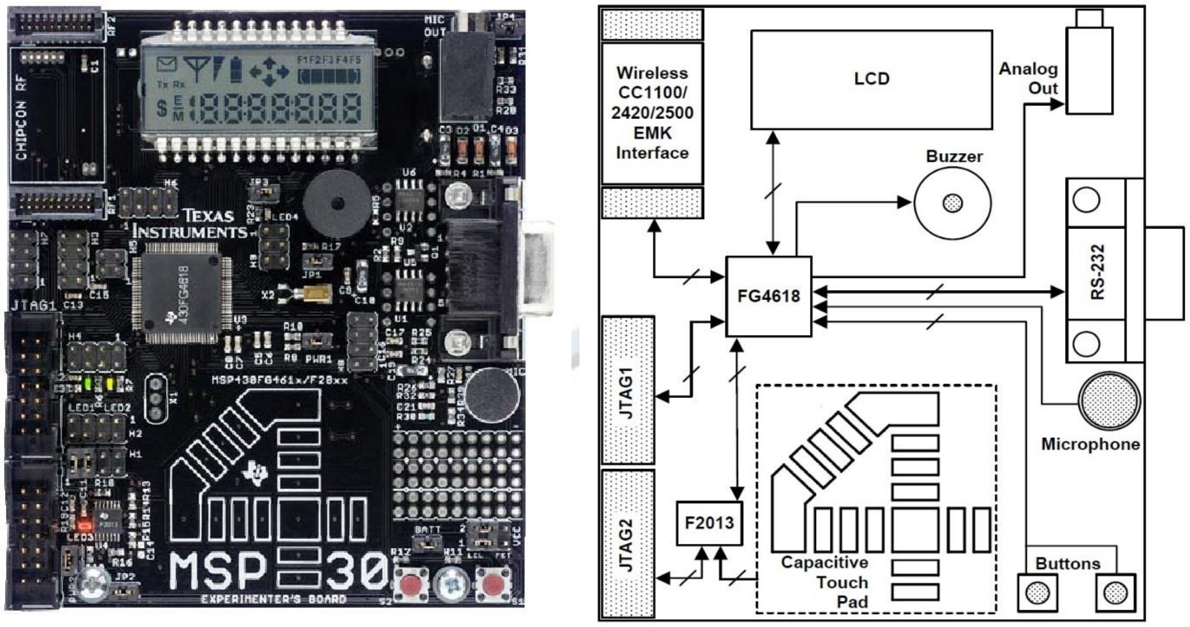
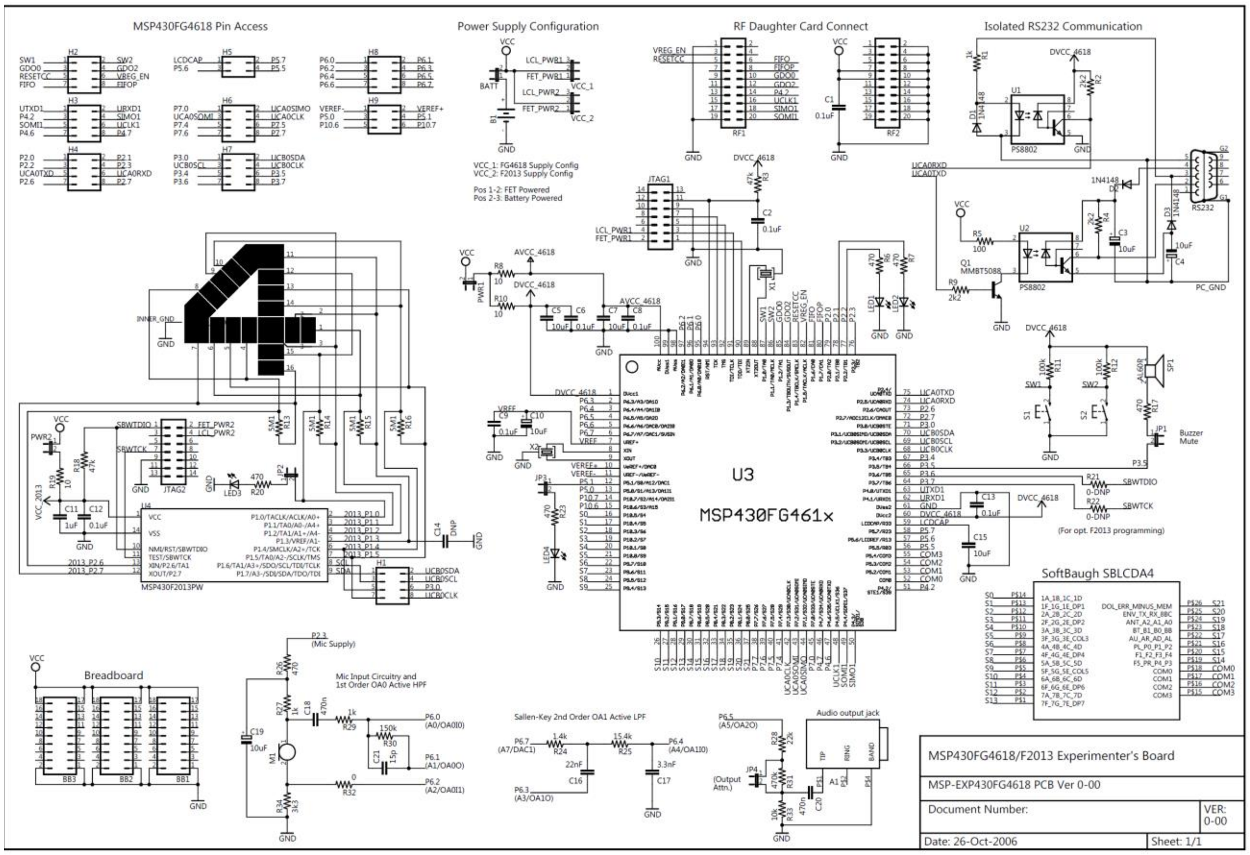


Figure 8. MSP430 Experimenter Board, Block Diagram.

To write software that utilizes external components, we will need to study the board schematics (Figure 9). For example, our first program will periodically toggle LED1 and LED2. The first step is to determine what port pins are connected to LED1 and LED2 and what we should do to turn them on or off. Notice that LED1 is connected to P2.2 via a 470 Ω resistor and LED2 is connected to P2.1 via another 470 Ω resistor. To have the LEDs on, the current needs to flow through the resistors, thus we need to provide a logic 1 on port pins P2.2 and P2.1. When the port pins are at a logic 0, there is no current flow and the LEDs are off. Consequently, by configuring port pins P2.2 and P2.1 to be standard digital outputs and periodically changing value in the register P2OUT (bits 2 and 1) we can toggle the LEDs. Code 1 shows the C source code for the program that toggles LED1 and LED2. Analyze the code and answer the following questions:

(a) What is the initial state of LED1 and LED2?
(b) How would you change the program so that LEDs are concurrently ON or OFF?
(c) What is the period of toggling?

(d) What happens if you comment out line 24 of the program?
(e) What happens if you change value of the variable *i* (smaller or larger than 50,000)?



MSP430FG4618 Pin Access
Power Supply Configuration
RF Daughter Card Connect
Isolated RS232 Communication
JTAG1
JTAG2
U3
MSP430FG461x
MSP430F2013PW
SoftBaugh SBLCDA4
Breadboard
Mic Input Circuitry and 1st Order OA0 Active HPF
Sallen-Key 2nd Order OA1 Active LPF
Audio output jack
MSP430FG4618/F2013 Experimenter's Board
MSP-EXP430FG4618 PCB Ver 0-00
Document Number:
VER: 0-00
Date: 26-Oct-2006
Sheet: 1/1

Figure 9. MSP430 Experimenter Board Schematic.

```
1    /*******************************************************************************
2    ;   TI Experimenter board demo, blinking leds LED1 and LED2 (MSP430FG4618)
3    ;
4    ;   Description: Toggle P2.1 and P2.2 by xoring P2.1 and P2.2 inside a loop.
5    ;                The leds are connected to P2.1 and P2.2 and are on when
6    ;                P2.1=1 and P2.2=1;
7    ;                The LEDs are initialized P2.1 to be off, and P2.2 to be on;
8    ;                ACLK = 32.768kHz, MCLK = SMCLK = default DCO
9    ;
10   ;                 MSP430xG461x
11   ;             -----------------
12   ;         /|\|                 |
13   ;          | |                 |
14   ;          --|RST              |
15   ;            |             P2.2|-->LED1(GREEN)
```

```
;             |             P2.1|-->LED2(YELLOW)
;
;   A. Milenkovic, milenka@uah.edu
******************************************************************************/
#include  <msp430xG46x.h>
void main(void)
{
   WDTCTL = WDTPW + WDTHOLD;   // Stop watchdog timer
   P2DIR |= 0x06;              // Set P2.1 and P2.2 to output direction (0000_0110)
   P2OUT = 0x02;               // Set P2OUT to 0000_0010b (LED2 is ON, LED1 is OFF)
     for (;;) {
     unsigned int i;
     P2OUT ^= 0x06;            // Toggle P2.1 and P2.2 using exclusive-OR
     i = 50000;                // Delay
     do (i--);
     while (i != 0);
   }
}

```

Code 1. Toggling the LEDs in C language (TI Experimenter's Board).